Area: III-V Compound Semiconductor and Space PV Technologies

ANNEALING EFFECTS ON GAAS/ITO/SI JUNCTIONS FABRICATED BY SURFACE-ACTIVATED BONDING

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I. Introduction

The surface-activated bonding (SAB) has enabled us to bond dissimilar materials with different lattice constants and thermal expansion coefficients to each other at low temperatures. The SAB, consequently, has successfully been applied for fabricating III-V/Si multi-junction solar cells. We previously reported on the performances of SAB-based InGaP/GaAs/ITO/Si hybrid triple-junction cell [1]. In this work, we fabricated GaAs/ITO/Si junctions by using the SAB and evaluated their electrical properties with the emphasis on the response to annealing so as to grasp the fundamental characteristics of ITO films as intermediate layers between III-V and Si subcells.

II. Experiments

A 90-nm-thick ITO film was deposited on an n^+-Si (100) substrate (doping concentration of ~2.6×10^{19} cm^3) by using the reactive plasma deposition. We also prepared an n^+-GaAs (epitaxial layer: 0.4 μm, ~2×10^{19} cm^3/n-GaAs (100) sub.) epitaxial substrate. Ohmic contacts were formed on the back surfaces of Si and GaAs substrates. Then 4mm^2 GaAs/ITO/Si junctions were fabricated by bonding these substrates and dicing. The GaAs/ITO/Si junctions were annealed at 100, 200, 300 and 400 ℃ for 300 s in N_2 gas ambient. We measured their current-voltage (I-V) characteristics at room temperature. We also observed their bonding interfaces by FE-SEM.

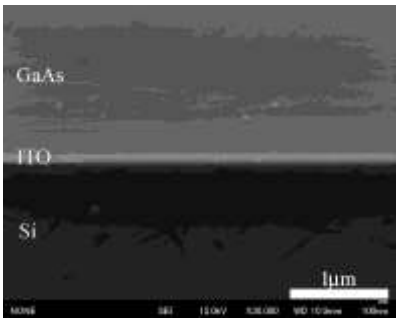

Fig.1 SEM image of GaAs/ITO/Si junctions

III. Results and discussions

Figure 1 shows a SEM image of the cross section of the GaAs/ITO/Si junction without annealing, which demonstrates that the interfaces with no voids were achieved. In Fig 2, the I-V characteristics of the annealed GaAs/ITO/Si junctions are compared with those of junctions without annealing. The interface resistances were found to be 0.11, 0.073, 0.080, 0.098 and 0.19 Ωcm^2 for the junctions without and with annealing at 100, 200, 300 and 400 ℃, respectively, by least-square fitting at 0 V. The interface resistance decreases with annealing at 100 ℃ and increases with annealing at higher temperatures. Similar behaviors were observed in I-V characteristics of annealed Si/ITO/Si junctions [2]. The obtained interface resistances were comparable to those of GaAs/Si junctions fabricated by using the SAB [3].

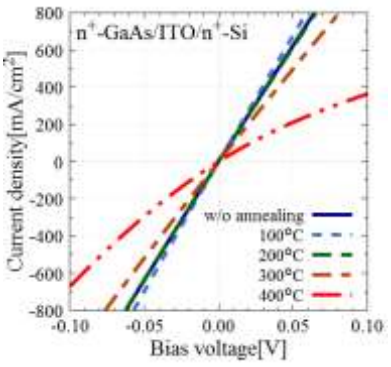

Fig.2 I-V characteristics of n^+-GaAs/ITO/n^+-Si junctions without and with annealing at 100, 200, 300 and 400 ℃

Acknowledgment

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Reference

[1] N. Shigekawa, et al. to be presented in PVSC-44 (2017)
[2] T. Ogawa, et al. presented in The 77th JSAP Autumn Meeting 15p-B10-17 (2016)
[3] J. Liang, et al. Jpn. J. Appl. Phys. 54 030211 (2015)