Japanese Journal of Applied Physics

The Japan Society of Applied Physics

REGULAR PAPER

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To cite this article: Takashi Hishida *et al* 2020 *Jpn. J. Appl. Phys.* **59** SBBB04

Japanese Journal of Applied Physics **59**, SBBB04 (2020) **REGULAR PAPER**
https://doi.org/10.7567/1347-4065/ab4c8a

Low-resistance semiconductor/semiconductor junctions with intermediate metal grids for III–V-on-Si multijunction solar cells

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Received July 12, 2019; revised September 9, 2019; accepted October 9, 2019; published online November 26, 2019

We fabricate semiconductor//metal grid/semiconductor junctions by using surface activated bonding (SAB) of heavily-doped Si and GaAs substrates to metal grids. The metal grids are self-aligned to SiO_2 layers on other Si substrates. The current–voltage characteristics of these junctions show linear properties. A low junction resistance of 1.99 mΩ cm^2 is achieved for an n^+-GaAs//metal grid/n^+-Si junction by successively annealing the junction at 300 °C for 1 h and 400 °C for 1 min in N_2 gas ambient. This value is much smaller than an interface resistance of SAB-based GaAs//ITO/Si junctions. These results demonstrate that metal grids could be useful for bonding subcells with low parasitic resistances in fabricating hybrid multijunction solar cells by SAB. © 2019 The Japan Society of Applied Physics

1. Introduction

III–V on Si multijunction solar cells are promising as next-generation solar cells since they can provide high efficiency with low cost in comparison with conventional Si and III–V multijunction cells.[1–3] Several authors previously fabricated III–V on Si multijunction solar cells by growing III–V subcells on Si-based bottom cells.[4,5] Although III–V (sub) cells were successfully grown on Si by using GaAsP-graded buffer layers[6] or Ge/Si templates,[7,8] the performance of the obtained III–V/Si cells were still limited because of the threading dislocations due to the difference in lattice constants between the III–V materials and Si.[5] III–V subcells are placed on Si bottom cell by alternative approaches such as the smart stack,[9] bonding of arrays of Au micropillars,[10,11] direct fusion bonding[12,13] and surface-activated bonding (SAB).[14–18] Among these approaches, the bonding of Au micropillars has been widely used in packaging of electronics and microelectromechanical systems although facilities for the alignments are needed at the step of bonding. The direct fusion bonding has also been applicable for fabricating junctions because of its simplicity. It should be noted, however, that in this bonding method a wet process is employed and annealing at temperatures higher than those in conventional III–V device process is essential for realizing interfaces with low electrical resistance.

In the SAB,[19–22] the surfaces of the substrates are irradiated by the fast atom beam (FAB) of Ar. Then the native oxide layers on the surface of the substrates are removed, or the surface are activated. In the next step, the substrates are weighted at room temperature. Using SAB, dissimilar semiconductor substrates with different lattice constants and thermal expansion coefficients can be directly bonded to each other without heating. We successfully fabricated InGaP/GaAs//Si triple-junction (3J) cells by using the SAB and achieved a conversion efficiency of ∼26%.[16]

The bonding interfaces with lower interface resistances are strongly required so as to achieve better performance of hybrid multijunction cells. The electrical conductivity of the bonding interface was improved by increasing the doping concentration of the bonding layers.[23] In addition, it was reported that the interface resistance of SAB-based junctions was decreased by annealing at low temperatures since damages introduced at the bonding interface due to the FAB irradiation were partially eliminated.[24–27] However, the interface resistance of SAB-based GaAs//Si junctions[24] is still larger than that of the lattice-matched III–V/IV interface (∼0.1 mΩ cm^2) formed by epitaxial growth[28] although the bonding condition was optimized.

We estimated the resistance across p^+-GaAs/n^+-Si bonding interface in actual 3J cells by characterizing cells with extra tap contacts connected to the p^+-GaAs and n^+-Si bonding layers.[16] The obtained resistance, ∼4 Ω cm^2, was much higher than the resistance of SAB-based junctions of p^+-GaAs and n^+-Si substrates (0.20 Ω cm^2).[25] An explanation for such a high resistance was that the thickness of the n^+-Si bonding layer, which also worked as emitters of bottom cells, was ∼10 nm, and the impacts of FAB irradiation manifested themselves more apparently in comparison with junctions of heavily-doped substrates.

A practical solution for the higher resistance in the bonding interface of 3J cells might be provided by forming conductive transparent film as intermediate layers on Si bottom cells and fabricating GaAs//intermediate layer/Si junctions. Lower series resistances are likely to be achieved by employing intermediate layers with higher conductivities (larger carrier concentration) than the emitter layers of Si bottom cells. The passivation effects of intermediate layers are also assumed to prevent the increase of resistance due to the FAB irradiation. We previously used indium tin oxide (ITO) films as intermediate layers and fabricated Si//ITO/Si and GaAs//ITO/Si junctions as well as InGaP/GaAs//ITO/Si 3J cells.[29–31] We found that the series resistance of InGaP/GaAs//ITO/Si 3Js was lower and their conversion efficiency was higher in comparison with InGaP/GaAs//Si 3Js. It is also found, however, that the resistance of GaAs//ITO/Si junctions increased by annealing them. Furthermore, the external quantum efficiency of Si bottom cells was lowered by inserting the ITO layers because of the optical properties of ITO.

These problems are assumed to be avoided by using metal grid in combination with dielectric materials such as SiO_2 and SiN. Figure 1 shows a schematic process for fabricating III–V/metal grid/Si 3J cells. Metal grid structures work as ohmic contacts for both of III–V and Si layers. Dielectric materials, such as SiO_2 and SiN, and metal grids are likely to protect Si surfaces. The metal grids must be slightly thicker than the dielectric materials so as to ensure successful

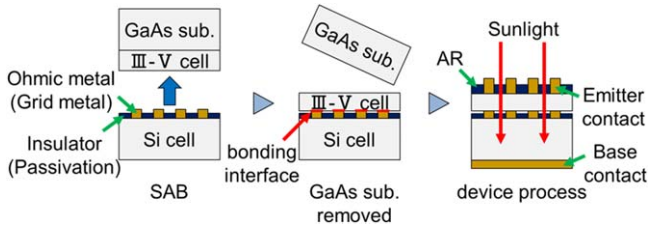

Fig. 1. (Color online) A schematic image of fabricating process of III–V/metal grid/Si 3J cells.

bonding of semiconductor to metal grid. It is also notable that impacts of shadow loss due to the metal grid can be minimized by aligning the emitter contacts on the top cells to the metal grids. We recently fabricated Si//metal grid/Si and GaAs//metal grid/Si junctions by SAB and reported on their current–voltage (I–V) characteristics.[32,33] In this paper, as an extension to previous works,[32,33] we focus on the electrical properties of semiconductor//metal grid junctions and show the possibility of application of metal grids for bonding subcells in fabricating hybrid multijunction cells.

2. Experimental methods

We used n^+-Si (100), p^+-Si (100) substrates as well as an n^+-GaAs/n-GaAs epitaxial substrate in this work. The resistivity and concentration of donors (N_D) were found to be 1.2 mΩ cm and $7.4 \times 10^{19}\,\mathrm{cm}^{-3}$ for the n^+-Si (100) substrates by Hall measurements. The resistivity and concentration of acceptors for the p^+-Si (100) substrates were estimated to be 3.1 mΩ cm and $5.7 \times 10^{19}\,\mathrm{cm}^{-3}$, respectively. The GaAs epitaxial substrate was composed of a 400 nm thick n^+-GaAs epitaxial layers ($N_D \sim 1 \times 10^{19}\,\mathrm{cm}^{-3}$) on an n-GaAs (100) substrates with $N_D \sim 1 \times 10^{18}\,\mathrm{cm}^{-3}$. Al/Ni/Au, Ti/Au, and AuGe/Ni/Au multilayers were evaporated on the backside surfaces of the p^+-Si, n^+-Si, and n^+-GaAs/n-GaAs substrates, respectively. The ohmic contacts on backsides surfaces of p^+-Si and n^+-GaAs were formed by annealing them at 400 °C for 1 min in N_2 gas ambient.

70–80 nm thick SiO_2 passivating layers were formed on the surface of the Si substrates by the RF magnetron sputtering. Self-aligned metal grids, which were parts of Si//metal grid/Si junctions, were fabricated by etching the SiO_2 layer using a buffered HF, evaporating Al (100 nm) layers and lift-off. Ti (60 nm)/Ni (15 nm)/Au (10 nm)/Ge (8 nm)/Au (18 nm) multilayers were used as substitute for the Al layer in case of fabricating n^+-GaAs//metal grid/Si junctions. Note that materials of grid metal were selected so as to form ohmic contacts to the respective bonded substrates.[34] The width and gap of grid were 20 and 180 μm, respectively. The coverage to the substrate by the metal grid was 25.2%, which was close to the coverage by emitter contacts on a commercially available III–V/Ge 3J cell. A top view of the metal grid is shown in Fig. 2.

We bonded the metal grid to the Si and GaAs substrates by using the SAB at 200 °C and fabricated p^+-Si//metal grid/p^+-Si, p^+-Si//metal grid/n^+-Si, n^+-Si//metal grid/n^+-Si, n^+-GaAs//metal grid/n^+-Si junctions. In addition, we fabricated directly bonded n^+-GaAs//n^+-Si junctions for comparison with n^+-GaAs//metal grid/n^+-Si junctions. All the samples were diced into 4 mm^2 pieces. A photograph of a

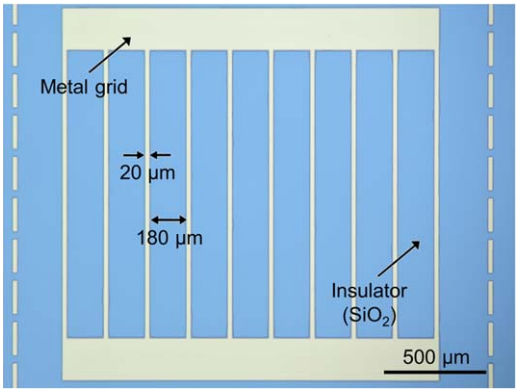

Fig. 2. (Color online) A microscope image of a metal grid self-aligned to a SiO_2 layer on a Si substrate.

Si//metal grid/ Si junction after dicing is shown in Fig. 3. The entire process sequence for fabricating samples is schematically shown in Fig. 4.

I–V characteristics were measured by using an Agilent B2902A Precision Measurement Unit at room temperature. I–V characteristics of the respective Si//metal grid/Si junctions were measured before and after the post-bonding annealing at 300 °C for 1 min, 300 °C for 1 h, and 400 °C for 1 min in N_2 gas ambient, respectively. Before measurement, n^+-GaAs//metal grid/n^+-Si and n^+-GaAs/n^+-Si junctions were annealed at 300 °C for 1 h and 400 °C for 1 min in N_2 gas ambient successively so as to form ohmic contacts of n^+-GaAs/metal grid.

In addition, we fabricated Si//metal grid (Al 500 nm)/Si, GaAs//metal (Ti (60 nm)/Ni (15 nm)/Au (10 nm)/Ge (8 nm)/Au (18 nm))/Si junctions. We observed their bonding interfaces using a field emission scanning electron microscope (FE-SEM) (JEOL JSM6500F).

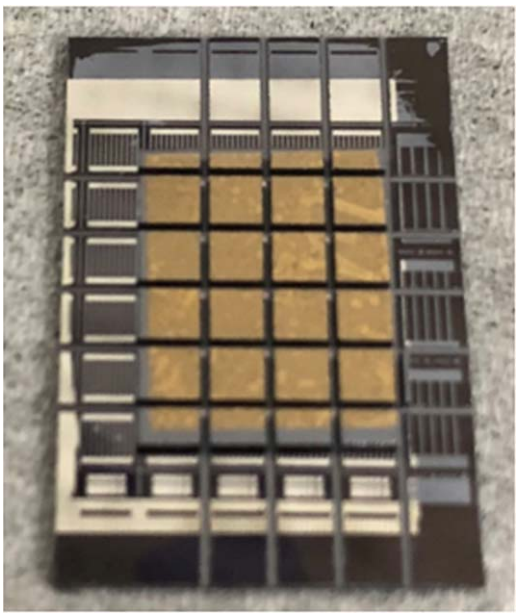

Fig. 3. (Color online) A photograph of a Si//metal grid/ Si junction after dicing.

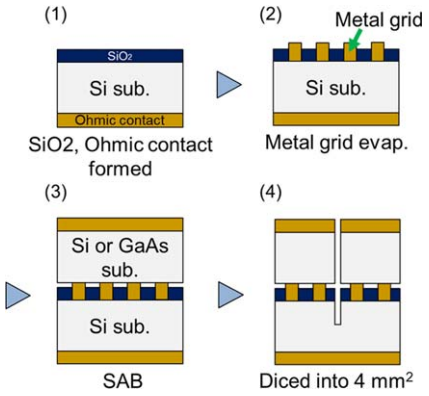

Fig. 4. (Color online) Process sequence for preparing of Si or GaAs//metal grid/Si junctions.

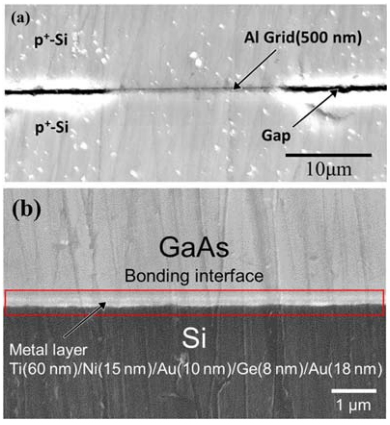

Fig. 5. (Color online) Cross-sectional FE-SEM images of (a) Si//metal grid/Si[32] and (b) GaAs//metal/Si interfaces.

3. Results and discussion

3.1. Results

Figures 5(a) and 5(b) show FE-SEM images of the cross section of the Si//metal grid/Si and GaAs//metal/Si junctions, respectively. As is shown in Fig. 5(a), the two SI substrates are successfully bonded to each other via the Al grid. It is also notable that ∼500 nm gaps were formed between the substrates. As is shown in Fig. 5(b), a GaAs//metal/Si junction was successfully fabricated, as with the Si//Al grid/Si junction.

Figure 6 shows typical *I*–*V* characteristics of p^+-Si//metal grid/p^+-Si, p^+-Si//metal grid/n^+-Si, and n^+-Si//metal grid/n^+-Si junctions measured between −0.03 and 0.03 V at room temperature before post-bonding annealing. Note that the current was normalized to a die area (4 mm^2). We found that all *I*–*V* characteristics shown in this figure revealed linear properties. The junction resistances were estimated to be 12.4, 12.0, and 1.19 mΩ cm^2 for p^+-Si//metal grid/p^+-Si, p^+-Si//metal grid/n^+-Si, and n^+-Si//metal grid/n^+-Si junctions, respectively, by least-squares fitting in the vicinity of 0 V.

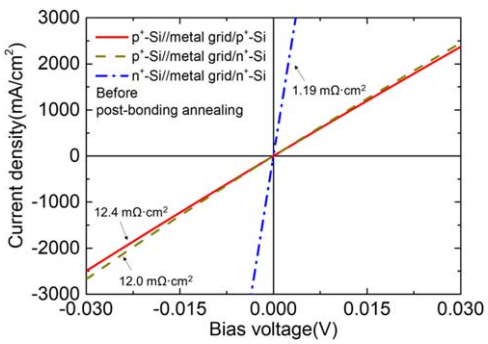

Fig. 6. (Color online) Room-temperature *I*–*V* characteristics of p^+-Si//metal grid/p^+-Si, p^+-Si//metal grid/n^+-Si, and n^+-Si//metal grid/n^+-Si junctions before post-bonding annealing.

Typical room-temperature *I*–*V* characteristics of p^+-Si//metal grid/p^+-Si, p^+-Si//metal grid/n^+-Si, and n^+-Si//metal grid/n^+-Si junctions before and after the post-bonding annealing are shown in Figs. 7(a)–7(c), respectively. We found that *I*–*V* characteristics of all junctions revealed linear properties. The relationship between junction resistances of all dies and annealing condition are shown in insets of the respective figures. The resistance of all type of junctions decreased by annealing at 300 °C, whereas annealing at 400 °C caused an increase in the resistance. The lowest junction resistance was 1–3 mΩ cm^2 irrespective of polarity of Si substrates. The spread of distribution of

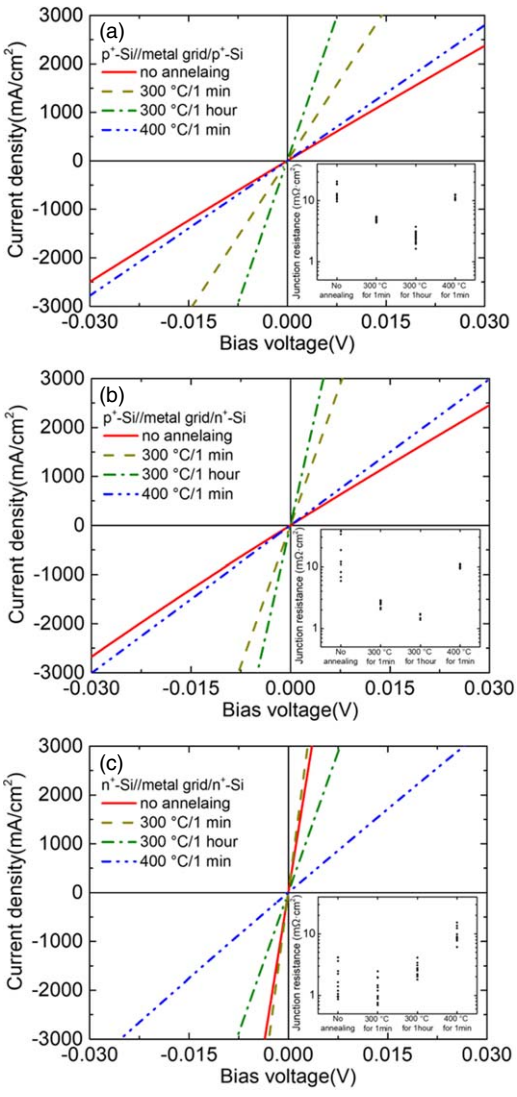

Fig. 7. (Color online) Room-temperature *I*–*V* characteristics of (a) p^+-Si//metal grid/p^+-Si, (b) p^+-Si//metal grid/n^+-Si, and (c) n^+-Si//metal grid/n^+-Si junctions with different post-bonding annealing. The inset shows the junction resistances of all dies.

junction resistance, which decreased by annealing at 300 °C, increased when the junctions were annealed at 400 °C.

Figure 8 shows the *I–V* characteristics of n^+-GaAs//metal grid/n^+-Si and n^+-GaAs/n^+-Si junctions at room temperature after post-bonding annealing. The *I–V* characteristics of these junctions also showed linear properties. The junction resistance for n^+-GaAs//metal grid/n^+-Si and n^+-GaAs/n^+-Si junctions were estimated to be 1.99 and 19.7 mΩ cm^2, respectively.

3.2. Discussion

In our previous work,[25] junction fabricated by directly bonding heavily-doped Si substrates revealed resistance of 34–206 mΩ cm^2. These resistance values are 3–10 times larger than the junction resistance of Si//metal grid/Si resistance (1.19–12.4 mΩ cm^2 as is seen from Fig. 6). From Figs. 7(a)–7(c), junction resistances of all Si//metal grid/Si junctions decreased by annealing at 300 °C. It is assumed that damages introduced at the bonding interface due to the FAB irradiation are partially eliminated by annealing.[24–27] The increase of junction resistances by annealing at 400 °C is considered to be due to the oxidation of the grid Al. In Fig. 9, we compare dependencies of the typical resistance of Si//ITO/Si junctions on the annealing temperature[29] with dependence of the resistance of junctions with metal grids. We find that the resistance of junctions with metal grids is ∼10 times smaller than the resistance of Si//ITO/Si junctions irrespective of the annealing temperature and polarity of Si substrates.

As with bonding of Si substrates, the junction resistance of n^+-GaAs//metal grid/n^+-Si resistance (1.99 mΩ cm^2) is smaller than the resistance of n^+-GaAs//n^+-Si (19.7 mΩ cm^2),[25] and n^+-GaAs//n^{++}-Si (3.6 mΩ cm^2)[24] junctions as well as n^+-GaAs//ITO/n^+-Si junction resistance (200 mΩ cm^2).[30] The usage of metal grids is likely to be promising for fabricating junctions with low parasitic resistances for III–V// Si multijunction cells. By assuming that their short-circuit currents (J_{sc}) are typically J_{sc} ∼0.01 A cm^{-2} for the incident solar power P_{inc} of $P_{inc} = 0.1$ W cm^{-2} (air mass 1.5 G/one sun), the impacts of the junction resistance $R_j = 1.9$ mΩ cm^2, the resistance observed for n^+-GaAs//metal grid/n^+-Si junctions, to the conversion efficiency $\Delta\eta$ should be

$$\Delta\eta = \frac{{J_{SC}}^2 R_j}{P_{inc}} \simeq 2 \times 10^{-6} = 2 \times 10^{-4}(\%), \quad (1)$$

which is assumed to be negligibly small. It is notable that junctions with negligible budget for efficiency of solar cells

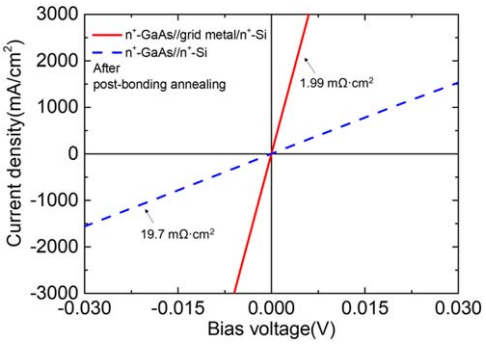

Fig. 8. (Color online) Room-temperature *I–V* characteristics of n^+-GaAs//metal grid/n^+-Si and n^+-GaAs//n^+-Si junctions after post-bonding annealing.

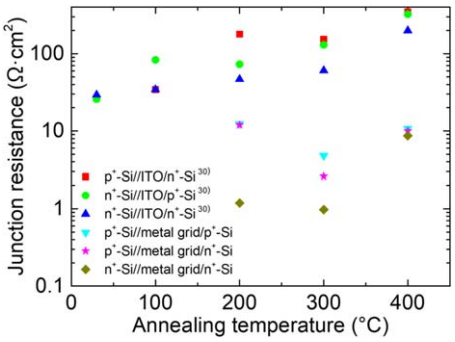

Fig. 9. (Color online) The typical resistance of Si//ITO/Si[29] and Si//metal grid/Si junctions as a function of annealing temperature.

are likely to be realized without using metal//metal bonding like micropillar-arrays Au–Au bonding.[10,11]

Here we assume that we can ignore the contribution of the substrate resistance and the contact resistance on the backside surfaces of bonded substrate to the measured resistance. On the assumption, we obtain the interface resistance by normalizing the measured resistance to the area of metal grids (0.01 cm^2). The estimated interface resistance is 3.11, 3.01, 0.299, and 0.300 mΩ cm^2 for the p^+-Si//metal grid/p^+-Si, p^+-Si//metal grid/n^+-Si, n^+-Si//n^+-Si and n^+-GaAs//metal grid/n^+-Si junctions, respectively. The interface resistance is assumed to be the sum of the contact resistance of evaporated metal (Al or Ti) layers on n^+- or p^+-Si substrates and the resistance of Si//metal or GaAs//metal bonding interface. In a preliminary study we observed that the resistance of Al-n^+-Si, Al-p^+-Si contacts were $<4 \times 10^{-2}$ mΩ cm^2 irrespective of the annealing condition. This finding, which agrees with other authors' reports that the contact resistance is as low as $<10^{-2}$ mΩ cm^2 for Al-n^+-Si, Al-p^+-Si, and Ti-n^+-Si contacts,[35,36] suggests that the interface resistance is mainly attributable to the resistance across the semiconductor//metal bonding interfaces. Their resistance is likely to be ∼3, 0.3, and 0.3 mΩ cm^2 for the p^+-Si//Al, n^+-Si//Al, and n^+-GaAs//Au-Ge junction, respectively.

4. Conclusions

We fabricated p^+-Si//metal grid/p^+-Si, p^+-Si//metal grid/n^+-Si, n^+-Si//metal grid/n^+-Si, and n^+-GaAs//metal grid/n^+-Si junctions by bonding metal grids evaporated on Si substrates to Si or GaAs substrates using SAB. The metal grids were self-aligned to SiO_2 passivating layers. Their electrical properties were investigated by measuring *I–V* characteristics at room temperature before and after the post-bonding annealing. The *I–V* characteristics of all junctions showed linear properties. The junction resistance before the post-bonding annealing was estimated to be 12.4, 12.0, and 1.19 mΩ cm^2 for p^+-Si//metal grid/p^+-Si, p^+-Si//metal grid/n^+-Si, and n^+-Si//metal grid/n^+-Si junctions, respectively. Annealing at 300 °C decreased the resistance of all junctions, whereas annealing at 400 °C increased the resistance of all junctions. The junction resistance of n^+-GaAs//metal grid/n^+-Si junction was found to be 1.99 mΩ cm^2. This junction resistance was smaller than the resistance of n^+-GaAs//n^+-Si, n^+-GaAs//ITO/n^+-Si junctions after the post-bonding annealing. The impacts of the junction resistance to the conversion efficiency of III–V

on Si multijunction solar cells was estimated to be as small as $\sim 2 \times 10^{-4}$%. These results demonstrated that metal grids could be useful for bonding subcells with low parasitic resistances in fabricating hybrid multijunction solar cells by SAB.

Acknowledgments

This work was supported by "Development of high performance and reliable PV modules to reduce levelized cost of energy" project of the New Energy and Industrial Technology Development Organization (NEDO) of Japan.

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