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Aluminum Foil/Si Direct Bonding as Prototypes of Ultra-Thick Metal Contacts in Devices

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We bonded aluminum (Al) foils to Si substrates to fabricate Al/p-Si, Al/n-Si, Al/p^+-Si, and Al/n^+-Si junctions by surface activated bonding (SAB) method and investigated the effects of the annealing process on the electrical properties of the junctions by measuring their current - voltage (*I-V*) characteristics. It was found that the leakage current of the reverse bias voltage in the bonded Al/n-Si junctions significantly decreased and the interface resistance of the bonded Al/p-Si junctions dramatically decreased with the annealing temperature. The smallest interface resistances of the bonded Al/p^+-Si and Al/n^+-Si junctions were obtained to be 0.021 and 0.032 $\Omega \cdot cm^2$, after annealing at 300 and 400°C, respectively. We demonstrated the fabrication of Al foil mesa-structures and micro wiring with complex structures on Si substrates. The sheet resistance of the bonded micro wiring was found to be more than two orders of magnitude lower than that of the evaporated micro wiring. In addition, Al foil mesa structures revealed a good thermal stability at the annealing temperature lower than 600°C. These results indicated that the fabrication of the thick metal electrode in devices could be realized by SAB.

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Ohmic contact to semiconductor would degrade substantially the overall performance of the high-power devices and circuits with large-current and/or high-voltage capability.[1] The major performance loss is usually due to the high ohmic contact resistance between metal electrode and semiconductor. Thus, the realization of excellent ohmic contact on semiconductor is absolutely necessary to obtain optimum device performance. The primary factors determining contact resistance are carrier concentration, semiconductor surface preparation and cleaning, and contact metal work functions hence Schottky barrier height.[2,3] In addition, it has been reported that the ohmic contact resistance decreased with increasing the metal thickness.[4] However, it is extremely difficult to obtain the deposition of the thick metal layer because it would take a large quantity of time and the production cost by the conventional coating method such as Electron-Beam-Evaporation and Sputter-Deposition. One way to circumvent these difficulties is surface-activated bonding (SAB),[5,6] in which different substrate materials could be directly bonded to each other without heating. We previously successfully fabricated Al/p-Si junctions by SAB and found that the current-voltage (I-V) characteristics of the bonded junctions revealed Schottky rectifying property.[7,8] The formation of ohmic contact generally requires a heat-treatment process so that the evaporated metals could react with the semiconductor to reduce the barrier height of the interface. Thus, to investigate the annealing temperature dependence of the electrical properties of the bonded Al/Si junctions is very necessary to realize the fabrication of the thick film metal electrode.

In this study, we demonstrated the fabrication of Al/p-Si, Al/n-Si, Al/p^+-Si, and Al/n^+-Si junctions by SAB method and examined the annealing temperature dependence of the electrical properties of the bonded junctions. The electrical properties of the bonded junctions without and with annealing at various temperatures were investigated by current-voltage (*I-V*) measurement and the feasibility of aluminum (Al) foil electrode was discussed. The Al 2p photoemission spectra of the bonded Al/Si junctions without and with annealing at various temperatures after removing Al were characterized by X-ray photoelectron spectroscopy (XPS). Furthermore, the structural properties of the bonding interfaces were examined by field emission-scanning electron microscopy (FE-SEM) and energy dispersive X-ray spectroscopy (EDS).

Experimental

Four types (p-, n-, p^+-, and n^+-) of (100) Si substrates and Al foils with the thickness of 17 μm (it is commercially available) are used for our bonding experiment. The carrier concentration of Si substrates and the information of Al foil are shown in Table I. The Al/Ni/Au and Ti/Au multilayers were evaporated on the back surface of p-Si and n-Si substrates, respectively, prior to the bonding. The ohmic contacts of p-Si substrates were achieved by a rapid thermal annealing process at 400°C for 1 min in N_2 gas ambient. In addition, Al electrode on both surfaces of p^+-Si and n^+-Si substrates were fabricated by evaporating Al/Au multilayers. Al foil was bonded to respective Si substrates by SAB,[5,6] so that Al/p-Si, Al/n-Si, Al/p^+-Si, and Al/n^+-Si junctions were obtained. It is noted that the bonding substrates were not heated during the bonding process. After the bonding, square mesa structures with the wide groove of 0.5 mm and the size of 1.6 × 1.6 mm^2, micro wiring structures with the length of 7000 μm and the width of 200, 150, 100, and 50 μm, and circular structures with the diameter of the inner and outer circles of 300 and 400 μm were fabricated on Si substrates by photolithography and wet etching processes. And then an Au layer with the thickness of 100 nm was evaporated on the surface of 1.6 × 1.6 mm^2 mesa structures. The fabrication processes of Al/Si junctions and Al structures on Si substrate are shown in Fig. 1. The top view photographs of Al square mesa micro wiring, and circular structures fabricated on Si substrates are shown in Figs. 2b, 2c, and 3, respectively. In addition, the micro wiring structures with the length of 7000 μm, the width of 200 μm, and the thickness of 200 nm were also fabricated on Si substrate by Al evaporating, photolithography, and wet etching processes. An Agilent B2902A Precision Measurement Unit was used for measuring the *I-V* measurements of the junctions with various annealing temperatures. Al diffusion at the bonded interface was evaluated before and after annealing at various temperature

Table I. The carrier concentration and the thickness of substrates.

Substrates/ foil	Carrier concentration (cm^{-3})	Thickness (μm)	Surface roughness (nm)
p-Si (100)	2.4×10^{17}	525	< 0.5
n-Si (100)	8.5×10^{15}	525	< 0.5
p^+-Si (100)	2.6×10^{19}	525	< 0.5
n^+-Si (100)	2.6×10^{19}	525	< 0.5
Aluminum foil (commercially available)		17	∼ several ten

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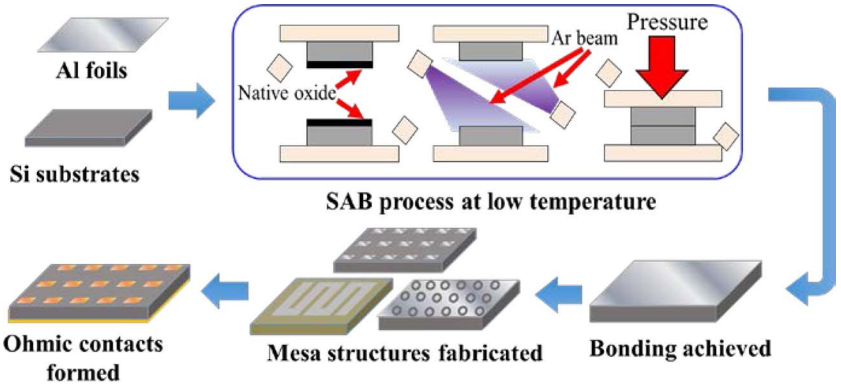


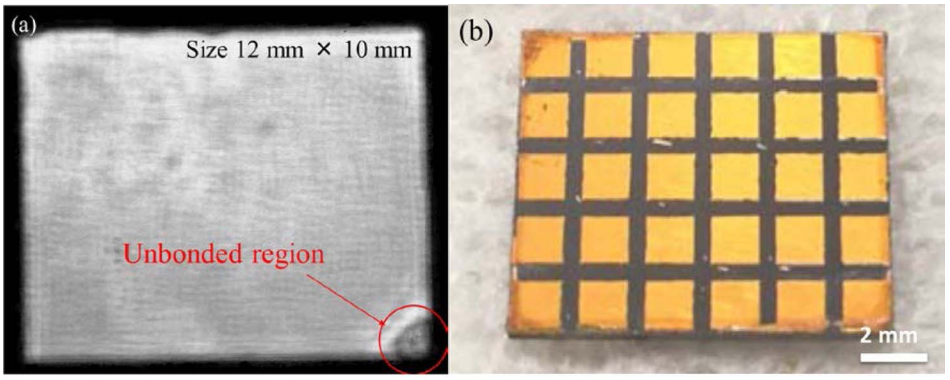
Figure 1. The fabrication processes of Al/Si junctions and Al structures on Si substrates.

by XPS (Shimadzu ESCA-3400) with a monochromatic Mg *K*α X-ray radiation source. The Al/Si bonded interfaces were investigated by FE-SEM facility (JEOL JSM6500F) equipped with an EDS apparatus and characterized for bonded area using a scanning acoustic microscopy with a 90 MHz transducer (HITACHI FineSAT).

Results and Discussion

The scanning acoustic microscopy image of the bonded Al/Si sample is shown in Fig. 2a. A small dark gray area was observed in the lower right corner of the sample, which corresponds to the unbonded area of Si and Al. However, in addition to this small unbonded area, no any voids were observed in the sample, which indicates that a large bonding area of Si and Al was achieved. Figures 2b and 2c show the photographs of Al foil square mesa and micro wiring structures fabricated on Si substrates, respectively. As shown in Figs. 2b and 2c, the complete and complex mesa and wiring structures were formed on Si substrates and no any defects were observed in the mesa structures. These results showed that Al foil could be applied to fabricate the complex pattern such as serpentine wiring

Figure 3 shows the *I-V* characteristics of the micro wirings with the length of 7000 μm and the width of 200 μm fabricated by evaporating and bonding, in which the thickness of the micro wiring fabricated by evaporating and bonding is 0.2 and 17 μm, respectively. Both the as-evaporated and bonded *I-V* characteristics reveal a linear property. The current density of the micro wiring was obtained by the



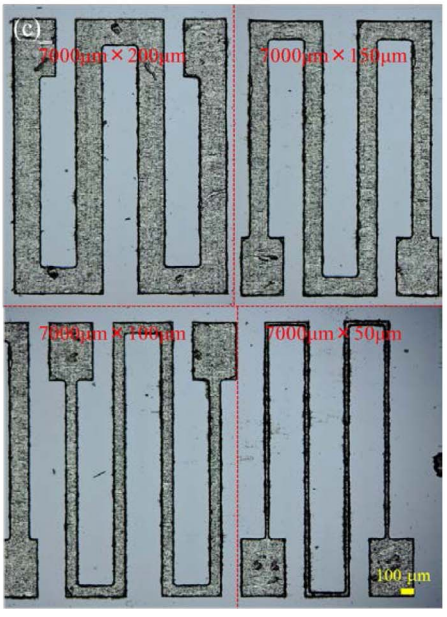


Figure 2. (a) A scanning acoustic microscopy image of Al/Si bonded sample, (b) Photograph of Al foil mesa-structures fabricated on Si substrates, and (c) Photograph of Al foil micro wiring with the length of 7000 μm and the width of 200, 150, 100, 50 μm fabricated on Si substrates.

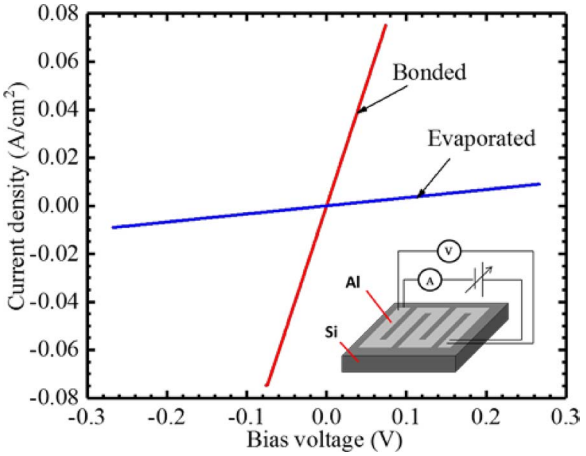


Figure 3. *I-V* characteristics of Al micro wiring with the length of 7000 μm and the width of 200 μm fabricated on Si substrate by evaporating and bonding. The thickness of the micro wiring fabricated by evaporating and bonding is 0.2 and 17 μm, respectively. The inset shows the schematic diagram of measurement.

measured currents were divided by the cross-section area of the micro wiring. The sheet resistance of the micro wiring fabricated by the evaporating and bonding was determined to be 4.23×10^{-1} and 2.12×10^{-3} Ω/square, respectively, from the *I-V* characteristics of the as-evaporated and bonded micro wirings. The resistance of the micro wiring fabricated by bonding is two orders of magnitude lower than that of the micro wiring fabricated by evaporating. This should be attributed to the reduction in the wiring's resistance due to the large cross-section area.

The photographs of Al circular mesa structures fabricated on Si substrates without and with annealing at 400, 500, 600, 800, and 1000°C are shown in Figs. 4a, 4b, 4c, 4d, 4e, and 4f, respectively. It was found that no drastic change is observed in the morphology of Al mesa structures for the annealing temperature lower than 600°C. When the annealing temperature increased from 600 to 800°C, the deformation of the surface morphology was observed on the mesa structures and the mesa isolation region was bulged. With increasing the annealing temperature up to 1000°C the morphological changes became more obvious, as shown in Fig. 4f.

Figures 5a and 5b show the *I-V* characteristics of the bonded Al/n-Si and Al/p-Si junctions without and with annealing at various temperatures ranging from 100 to 400°C measured at room temperature, respectively. As shown in Fig. 5a, the *I-V* characteristics of the bonded Al/n-Si junctions without and with annealing at various temperatures show rectifying property. The barrier height was determined to be 0.57, 0.58, 0.59, 0.66, and 0.78 for the junction without and with annealing at 100, 200, 300, and 400°C, respectively, by using the thermionic emission theory.[9,10] We found that the barrier height is heavily sensitive to the annealing temperature, which increases with increasing the annealing temperature. In addition, the magnitude of the forward bias current decreased with the annealing temperature, which should be attributed to the series contact resistance increase. The magnitude of the current at – 3 V significantly decreased from 2.7×10^{-2} to 5.0×10^{-4} A/cm^2 as the annealing temperature increased to 400°C. The obtained reverse bias current and barrier height for the respective junctions are shown in Table II.

As shown in Fig. 5b, the *I-V* characteristics of the bonded Al/p-Si junction without and with annealing at 100 and 200°C reveal rectifying property. The current density of the reverse bias voltage decreased as the annealing temperature increased up to 200°C. The *I-V* characteristics of the bonded junctions with annealing at 300 and 400°C show symmetric property. The interface resistances were extracted to be 0.73 and 0.26 Ω · cm^2 for the junction annealed at 300 and 400°C, respectively, by least-square fitting around 0 V. In addition, the interface resistances of the bonded junctions without and with annealing

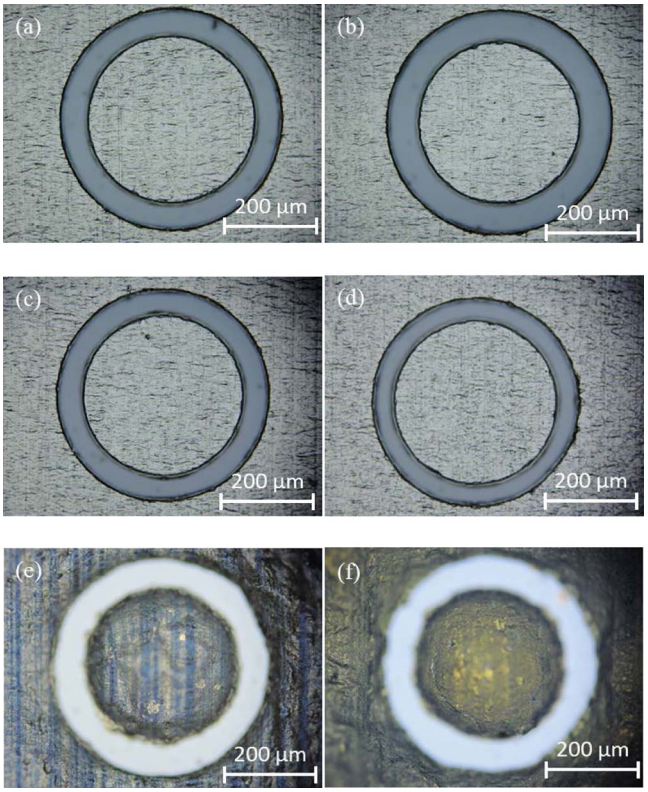


Figure 4. Photographs of Al circular mesa structures fabricated on Si substrate (a) without and with annealing at (b) 400, (c) 500, (d) 600, (e) 800, and (f) 1000°C.

at 100 and 200°C were also obtained in similar manners. The barrier height of the bonded junctions was fitted to be 0.62, 0.61, 0.62, 0.47, and 0.44 eV for the junctions without and with annealing at 100, 200, 300, and 400°C, respectively. Their interface resistances and barrier heights are shown in Table II. It was found that the interface resistance increased and the barrier height remained constant as the annealing temperature increased to 200°C and then decreased when the annealing temperature increased from 200 to 400°C.

The *I-V* characteristics of the bonded Al/p$^+$-Si junctions without and with annealing temperature between 100 to 400°C measured at room temperature are shown in Fig. 6a. We found that the *I-V* characteristics of the bonded junctions without and with annealing at 100 and 200°C showed nonlinear property. However, after annealing at 300 and 400°C, their *I-V* characteristics showed excellent linear property. Their interface resistances were found to be 0.021 and 0.042 Ω · cm^2 for the bonded junctions annealing at 300 and 400°C, respectively, by least-square fitting at approximately 0 V. In the same way, the resistances of the bonded junctions without and with annealing at 100 and 200°C were also obtained. The interface resistances of the bonded junctions with annealing at various temperatures are shown in Fig. 6b. To compare with the interface resistances of the bonded Al/p$^+$-Si junctions, the contact resistances of the evaporated Al electrode on p$^+$-Si substrates are also shown in Fig. 6b. It was found that the interface resistance of the bonded Al/p$^+$-Si junctions increased slightly as the annealing temperature increased up to 200°C, and then decreased sharply as the annealing temperature increased to 300°C, finally increased again when the temperature increased to 400°C. On the contrary, the contact resistance of the evaporated Al electrode on Si substrates almost remains constant after annealing at various temperatures.

Figure 7a shows the *I-V* characteristics of the bonded Al/n$^+$-Si junctions without and with annealing temperature between 100 to 600°C measured at room temperature. It was found that the *I-V* characteristics in this figure showed ohmic contact behavior. By least-squares

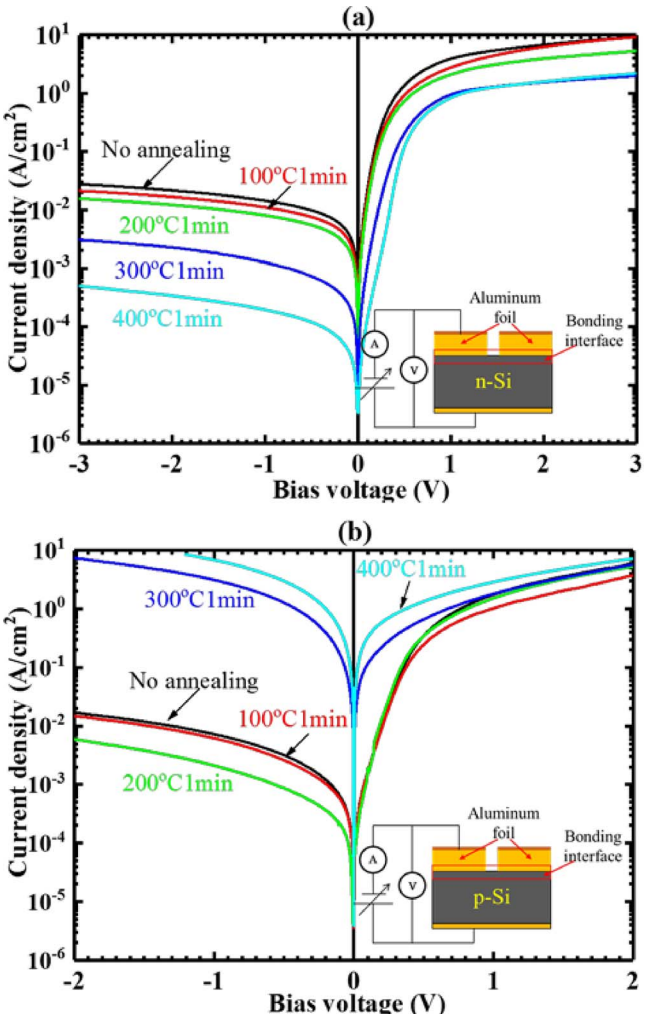


Figure 5. *I-V* characteristics of the bonded (a) Al/n-Si and (b) Al/p-Si junctions without and with annealing at various temperatures measured at room temperature. The inset shows the schematic diagram of measurement.

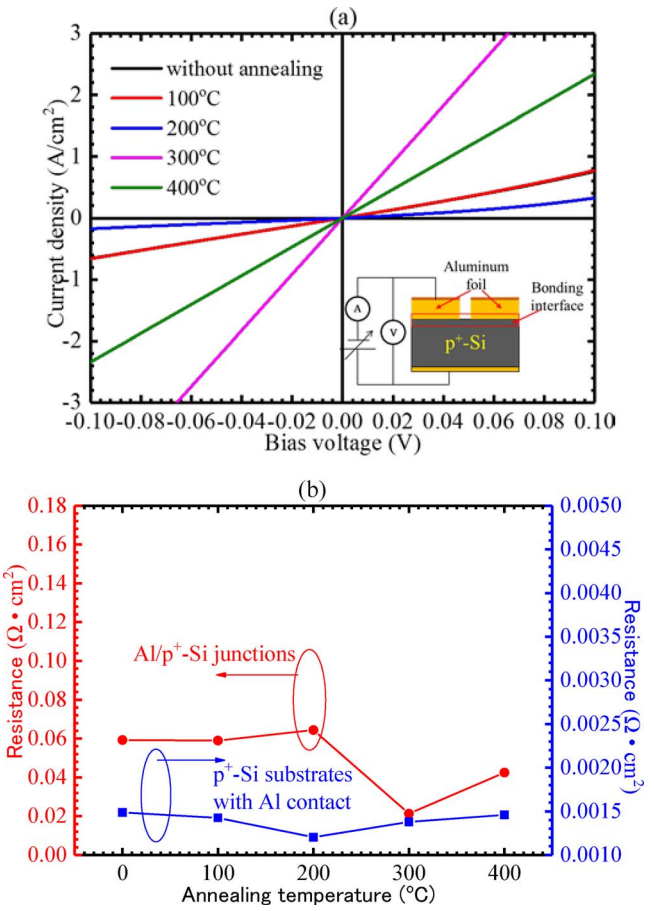


Figure 6. (a) *I-V* characteristics of the bonded Al/p^+-Si junctions without and with annealing at various temperatures measured at room temperature (Note that the data for without annealing overlaps with the data for annealing at 100°C) and (b) the interface resistances of the bonded Al/p^+-Si junctions and the contact resistances of the evaporated Al electrode on p^+-Si substrates as a function of the annealing temperature. The inset shows the schematic diagram of measurement.

fitting at approximately 0 V, the interface resistances of the bonded junctions without and with annealing at 100, 200, 300, 400, 500, 600°C were determined to be 0.04, 0.042, 0.038, 0.036, 0.032, 0.060, 0.167 $\Omega \cdot cm^2$, respectively, and are shown in Fig. 7b. In addition, the contact resistances of the evaporated Al electrode on n^+-Si substrates as a function of the annealing temperature are also shown in Fig. 7b. It is evident that the interface resistance of the bonded junctions decreased gradually as the annealing temperature increased up to 400°C and then increased substantially as the annealing temperature increased from 400 to 600°C. The resistance of the bonded junction with annealing at 400°C showed the lowest value in all bonded Al/n^+-Si junctions. Similar behaviors were also observed in the contact resistance of the evaporated Al electrode on n^+-Si substrates.

The Al 2p photoemission spectra of Si substrates that were prepared by annealing the bonded Al/Si samples at various temperatures and removing Al layer by Al wet etching are shown in Fig. 8. The fitting of Al 2p peak was performed with Gaussian function after the backgrounds were subtracted using Shirley's method. As shown in Fig. 8, the Al 2p spectrum of Si substrates with annealing at 800 and 1000°C was well fitted by a peak located at 76.2 eV, which can be assigned to the Al-O-Si bonding state.[11] A significant change of Al 2p spectra was observed in Si substrates after annealing temperature higher than 800°C. No any peaks related to Al 2p were observed after annealing at temperatures below 600°C.

Table II. The reverse-bias current and barrier height of the bonded Al/n-Si junctions and the interface resistance of the bonded Al/p-Si junctions with annealing at various temperatures.

	Al/n-Si junction		Al/p-Si junction	
Annealing temperature	Reverse-bias current (A/cm^2)	Barrier height (eV)	Resistance ($\Omega \cdot cm^2$)	Barrier height (eV)
Without annealing	2.7×10^{-2}	0.57	102.04	0.62
100°C	2.1×10^{-2}	0.58	109.89	0.61
200°C	1.6×10^{-2}	0.59	178.57	0.62
300°C	3.0×10^{-3}	0.66	0.73	0.47
400°C	5.0×10^{-4}	0.78	0.26	0.44

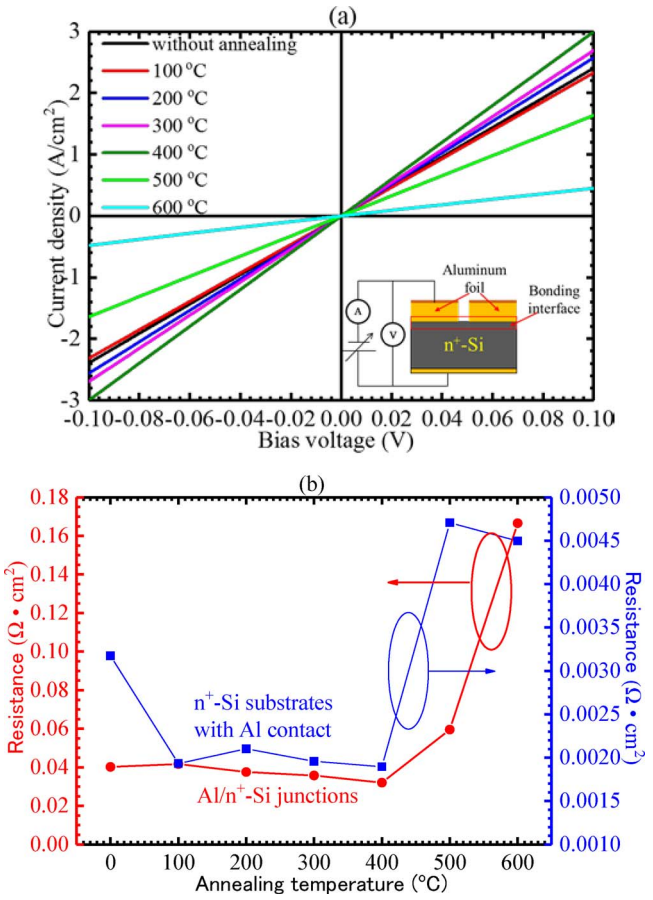


Figure 7. (a) *I-V* characteristics of the bonded Al/n$^+$-Si junctions without and with annealing at various temperatures measured at room temperature and (b) the contact resistances of the bonded Al/n$^+$-Si junctions and the contact resistances of the evaporated Al electrode on n$^+$-Si substrates as a function of the annealing temperature.

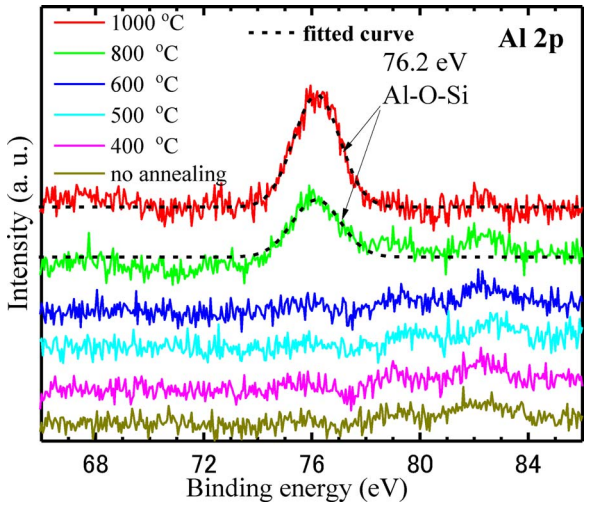


Figure 8. Al 2p photoemission spectra of Si substrates that were prepared by annealing the bonded Al/Si junctions at various temperatures and removing Al layer by wet etching.

The cross-sectional FE-SEM images of the bonded Al/Si interfaces without and with annealing at 1000°C for 1 and 10 min are shown in Figs. 9a, 9c, and 9e, respectively. A straight line can be clearly recognized at the center of the bonded interface without annealing, which corresponds to the bonded interface. After annealing at 1000°C for 1 and 10 min above the melting point of aluminum (660°C), instead of an abrupt interface a rough interface was observed at the bonded interfaces, which should be attributed to the inter-diffusion between Si and Al during high temperature annealing process. Furthermore, a ridge of Si diffused into Al region was observed at the interface. More importantly, no any cracks and interfacial delamination were observed at the bonded interface even after annealing at 1000°C. To investigate the microscale inter-reaction between Al and Si at bonded interface with annealing at 1000°C, SEM/EDX-based elemental mapping images of Figs. 9a, 9c, and 9e for element Al were examined and shown in Figs. 9b, 9d, and 9f, respectively. The distribution of Si and Al elements was indicated by different colors. As shown in Fig. 9b, no inter-diffusion was observed at the bonded interface without annealing, which is coincide with the SEM image. On the contrast, after annealing at 1000°C, the diffusion of Si into Al was observed at the bonded interface. Furthermore, with increasing annealing time the depth of the diffusion of Si increased.

It is worthy to note that (1) the contact resistance and the barrier height increased in the bonded Al/n-Si junctions and (2) the barrier height of the bonded Al/p-Si junctions decreased with the annealing temperature and (3) the interface resistance of the bonded Al/n$^+$-Si junctions increased after annealing at higher than 400°C, which suggest that the influence of annealing temperature on the electrical properties of the bonded Al/Si junctions should be related to the diffusion behavior of Al in Si substrates. It has been reported that the increase of the barrier height in n-Si Schottky diodes was due to a pn junction formed at the interface by Al atom as an acceptor impurity diffused into the n-Si substates.[12,13] Al components diffused into Si would neutralize (accelerate increase) the impurities of n-Si (p-Si) to increase (decrease) the contact resistance in n-Si (p-Si) substrates. The neutralization of Al acceptor and donor impurities has also reported in multi-crystalline silicon.[14] The abovementioned electrical properties of the bonded Al/n-Si and Al/p-Si junctions are also consistent with Al diffusion behavior in Si substrates during annealing process.

If a pn junction is formed on n$^+$-Si substrates during the annealing process, which should induce the increase of the interface resistance in the bonded Al/n$^+$-Si junctions and the contact resistance of the evaporated Al electrode on n$^+$-Si substrates. However, such increases were not observed in the bonded Al/n$^+$-Si junction and the evaporated Al electrode on n$^+$-Si substrates after annealing at lower than 400°C. Furthermore, Al components diffused into Si substrates were not detected in the Al 2p photoemission spectra of the bonded Al/Si junctions. It may be due to the concentration of Al component diffused into Si substrates is below the resolution of XPS equipment. Because the solubility level of Al in Si is about 1×10^{18} cm^{-3} at temperature lower than 550°C,[15] which is below the detection limit of XPS. Consequently, we can conclude that the concentration of Al component diffused into Si substrates should be too low to affect the conductivity of n$^+$-Si substrates when the annealing temperature is lower than 400°C.

After annealing temperature higher than 800°C, Al component was detected in the Al 2p photoemission spectra and SEM/EDX-based elemental mapping images of the bonded Al/Si interfaces. Furthermore, both the interface of the bonded Al/n$^+$-Si junctions and the contact resistance of the evaporated Al electrode on n$^+$-Si substrates significantly increased as the annealing temperature increased from 400 to 600°C. These results suggest that the increase in the interface resistance of the bonded Al/n$^+$-Si junctions and the contact resistance of the evaporated Al electrode on n$^+$-Si substrates should be due to the concentration of Al components diffused into Si substrates increases with increasing the annealing temperature.

For the bonded Al/Si junctions and the evaporated Al electrode on Si substrates, we observed a large discrepancy between the interface resistance and the contact resistance in the *I-V* characteristics. Such discrepancies should be related to the interface states formed at the bonded interface. In the present work, the Ar plasma irradiation in the SAB process is assumed to induce the interface sates. According

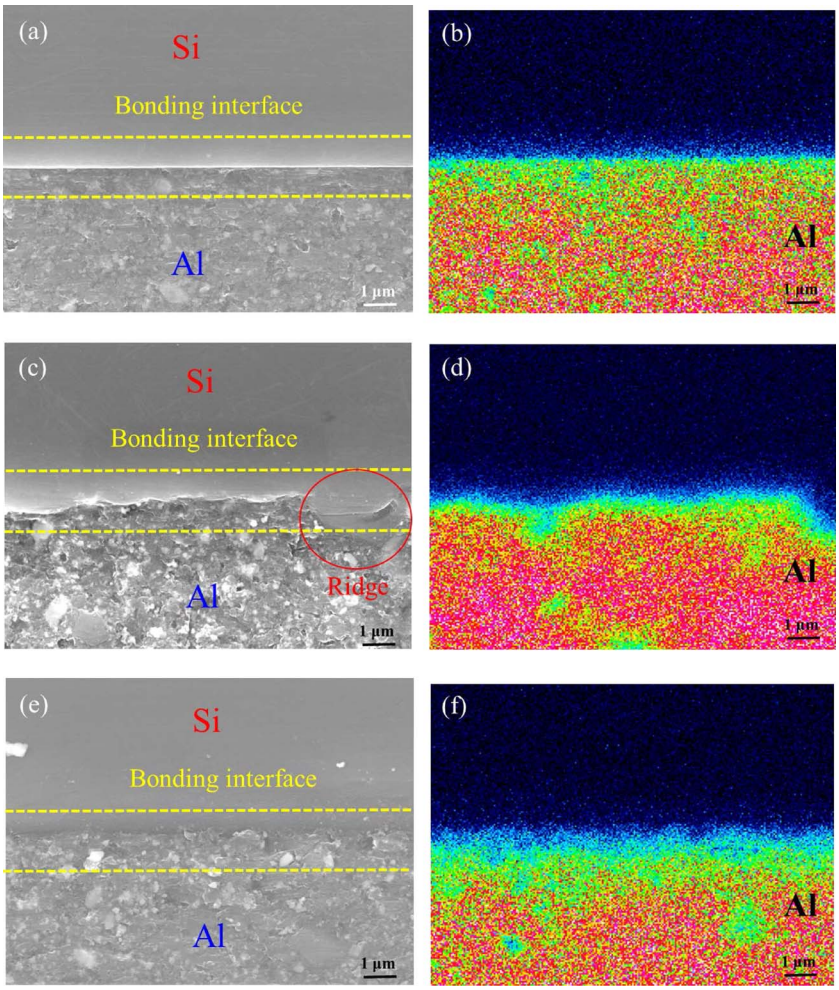


Figure 9. Cross-sectional FE-SEM images of the bonded Al/Si interfaces (a) without and with annealing at 1000°C for (c) 1 min and (e) 10 min. Results of the SEM/EDX-based elemental mapping of (b), (d), and (f) for (a), (c), and (e), respectively, for element Al.

to our previously reported on Si/SiC and Si/Si junctions fabricated by SAB,[16,17] a large number of interface states were formed at the bonded interface. The interface states would produce a potential barrier and depletion layers neighboring the bonding interface to degrade the transport properties of carriers across the bonding interfaces. Similar result has also been reported in p-Si and n-Si Schottky diodes, in which high density of interface states were generated by Ar ion implantation.[18,19]

It has been reported that the interface state density depended on the post annealing process for Si/Si and Si/GaAs junctions fabricated by SAB, which decreased as the annealing temperature increased.[17,20] The interface state density at the bonded Si/Si interface reduced to the smallest value after annealing at 1000°C. Therefore, the annealing process with high temperature may be required for reducing the interface resistance of the bonded Al/Si junctions. Moreover, it should be more suitable for the bonded Al/p-Si junctions by taking into consideration the effect of Al component diffusion into n-Si substrates.

Although the interface resistance value of the bonded Al/p^+-Si and Al/n^+-Si junctions is about one order of magnitude higher than that of the contact resistance of the evaporated Al electrode on p^+-Si and n^+-Si substrates, the sheet resistance of the micro wiring fabricated by SAB is more than two orders of magnitude lower than that of the conventional evaporated micro wiring on Si substrates. In addition, the interface resistance of the bonded Al/p^+-Si and Al/n^+-Si junctions is likely be reduced by optimizing the condition of SAB process and post-bonding annealing. It was demonstrated that Al foil could be applied to fabricate the thick metal mesa and complex micro wiring structures. The abovementioned results indicate that the ultra-thick metal electrode with low resistance contacts and high speed fabrication on semiconductors could be realized by using SAB method.

Conclusions

Al/n-Si, Al/p-Si, Al/n^+-Si, and Al/p^+-Si junctions were fabricated by SAB method and the effects of the annealing temperature on their electrical properties were investigated. The optimum annealing temperature has produced a marked improvement in the *I-V* characteristics of the bonded Al/n-Si, Al/p-Si, Al/n^+-Si, and Al/p^+-Si junctions. The barrier height of the bonded Al/n-Si junctions increased with the annealing temperature and increased to 0.78 eV after annealing at 400°C. In contrast, the barrier height of the bonded Al/p-Si junctions decreased with increasing annealing temperature and reduced to 0.44 eV after the junctions annealing at 400°C. The smallest interface resistances of the bonded Al/n^+-Si and Al/p^+-Si junctions were found to be 0.032 and 0.021 $\Omega \cdot cm^2$ after the junctions annealing at 400 and 300°C, respectively. The sheet resistance of the micro wiring fabricated by SAB is much more less than that of the evaporated micro wiring. In addition, the deformation of Al foil mesa structures annealed at lower than 600°C was not observed. The micro wiring with the length of 7000 μm and the width of 200, 150, 100, 50 μm were perfectly fabricated on Si substrates, which demonstrated that Al foil has potential application for the fabrication of thick metal electrode with the complex structure in device. These results indicated that SAB method is an effective way for fabricating thick film electrode with a thickness of several-ten micrometers.

Acknowledgments

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