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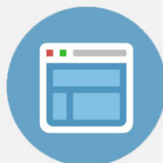

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Electrical properties of Si/Si interfaces by using surface-activated bonding

J. Liang,[a] T. Miyazaki, M. Morimoto, S. Nishida, and N. Shigekawa
Department of Electrical Engineering, Osaka City University, 3-3-138 Sugimoto, Sumiyoshi-ku, Osaka 558-8585, Japan

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Electrical properties of *n*-Si/*n*-Si, *p*-Si/*n*-Si, and p^--Si/n^+-Si junctions fabricated by using surface-activated-bonding are investigated. The transmission electron microscopy/energy dispersive X-ray spectroscopy of the *n*-Si/*n*-Si interfaces reveals no evidence of oxide layers at the interfaces. From the current-voltage (*I-V*) and the capacitance-voltage (*C-V*) characteristics of the *p*-Si/*n*-Si and p^--Si/n^+-Si junctions, it is found that the interface states, likely to have formed due to the surface activation process using Ar plasma, have a more marked impact on the electrical properties of the *p*-Si/*n*-Si junctions. An analysis of the temperature dependence of the *I-V* characteristics indicates that the properties of carrier transport across the bonding interfaces for reverse-bias voltages in the *p*-Si/*n*-Si and p^--Si/n^+-Si junctions can be explained using the trap-assisted-tunneling and Frenkel-Poole models, respectively. © *2013 AIP Publishing LLC*.
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I. INTRODUCTION

Direct wafer bonding, in which two wafers are bonded to each other without adhesive or solder, has been widely applied for fabricating a variety of heterogeneous structures, such as Si/Si,[1] Si/SiO_2,[2,3] GaAs/Si,[4] InP/Si,[5] GaAs/GaAs,[6] and GaAs/InP[7,8] because it enables us to form junctions of semiconductor materials with different crystal structures or lattice constants. In almost all direct bonding methods—hydrophilic, hydrophobic, plasma-assisted bonding, and others[9–11]—annealing after the bonding has been reported to be essential in achieving sufficient bonding strengths.[6–8,12] However, the fact that the need for annealing may limit the area of application of the direct wafer bonding, because the resultant thermal stress could cause the diffusion of doped impurities across the bonding interfaces. In addition, mechanical defects could occur at the bonding interfaces when junctions are made of materials with different thermal expansion coefficients.

On the other hand, surface-activated bonding (SAB),[13–18] in which substrates are attached to each other after their surfaces are activated by Ar plasma,[13] has been used for packaging semiconductor devices that are sensitive to thermal stress because there is no need to heat samples during the bonding process. Consequently, the mechanical and structural properties of SAB-based junctions have been investigated in the relevant research.[15,16] SAB is also applicable for fabricating junctions of dissimilar semiconductor materials with different thermal expansion coefficients as well as different crystal structures and lattice constants, and several results of *I-V* measurements have been reported for Si/Si, Si/InP, and Si/GaAs junctions fabricated by SAB.[14,17,18]

In this work, we fabricated *n*-Si/*n*-Si, *p*-Si/*n*-Si, and p^--Si/n^+-Si junctions using SAB and performed *I-V* and *C-V* measurements to examine their electrical properties. Mechanisms of carrier transport across the bonding interfaces in the *p*-Si/*n*-Si and p^--Si/n^+-Si junctions were investigated by analyzing the ambient temperature dependence of their *I-V* characteristics. The structural properties of the bonding interfaces were examined by transmission electron microscopy (TEM) and energy dispersive X-ray spectroscopy (EDS) observations of the *n*-Si/*n*-Si junctions.

II. EXPERIMENTS

A. Method

The *n*-Si/*n*-Si, *p*-Si/*n*-Si, and p^--Si/n^+-Si junctions were made of four types (*p*-, *n*-, p^--, and n^+-) of (100) Si substrates. Their carrier concentrations of the substrates, were estimated by Hall measurements at room temperature, are shown in Table I. To activate the sample surfaces, we used fast atom beams of Ar at the current of 1.8 mA and voltage ~2 kV for 180 s. After the bonding, ohmic contacts were prepared on the *p*- and p^--type (*n*- and n^+-type) Si substrates by evaporating Al/Ni/Au (Ti/Au) multilayers on their backsides. The *p*- and p^--type substrates were annealed at 400 °C for 60 s after the evaporation to obtain good contact characteristics. All the samples were diced into 4 mm^2 pieces.

I-V and *C-V* characteristics were measured with an ADCMT 6242 Source Measurement and an Agilent E4980A Precision Impedance Analyzer, respectively. The bonding interfaces of the *n*-Si/*n*-Si junctions were observed with TEM (Hitachi H9000UHR) equipped with an EDS apparatus.

B. Results

Figure 1(a) shows a TEM image of the *n*-Si/*n*-Si interface. A transition layer with thickness estimated to be 9 nm was formed at the interface. More importantly, no structural defects such as cracks were observed at the interface. Figure 1(b) shows EDS results for the upper *n*-Si substrate, inside the transition layer, and the lower *n*-Si substrate. The areas

[a]Electronic email: liang@elec.eng.osaka-cu.ac.jp

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TABLE I. The resistivity, the carrier concentration, and the thickness of substrates.

Type	Resistivity Ω·cm	Carrier concentration cm^{-3}	Thickness cm
p-Si(100)	0.02	8.7×10^{18}	0.0328
n-Si(100)	0.02	2.5×10^{18}	0.0328
P^{-}-Si(100)	0.1	2.4×10^{17}	0.0525
n^{+}-Si(100)	0.002	2.6×10^{19}	0.0525

for the respective EDS observations are marked a1, a2, a3, a4, and a5 in Fig. 1(a), where a2–a4 are inside of the transition layers and a1 and a5 are separated from the interface by approximately 12 nm. The atomic ratio of oxygen extracted from areas a3 (1.9%) and a4 (1.8%) are similar to that for area a1 (1.8%). The atomic ratio of oxygen for area a2 (0.8%) is smaller than that for area a1 (1.8%), while it is close to that for area a5 (0.7%). Note that signals from Cr, Fe, and Ag atoms are observed in the EDS spectra for areas a2–a4.These elements are probably contaminants that formed during the activation process. No signals due to Ar atoms are observed in any of the EDS spectra.

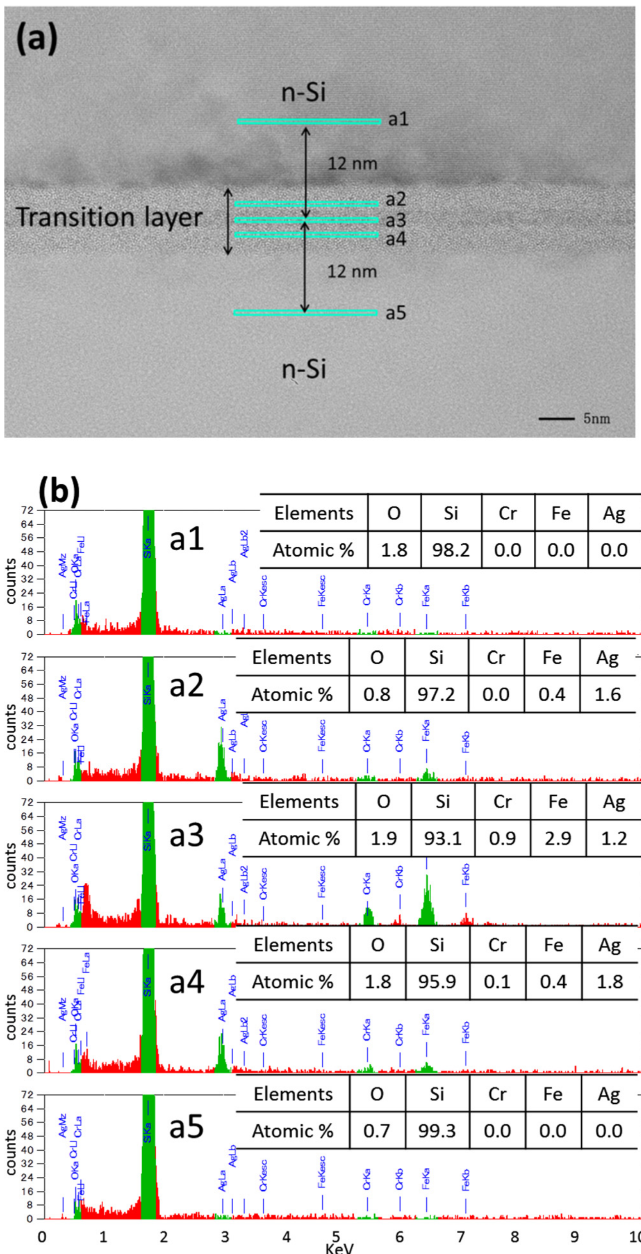

FIG. 1. (a) TEM cross-section image of the interface of *n*-Si/*n*-Si and (b) EDS composition maps of the interface of *n*-Si/*n*-Si.

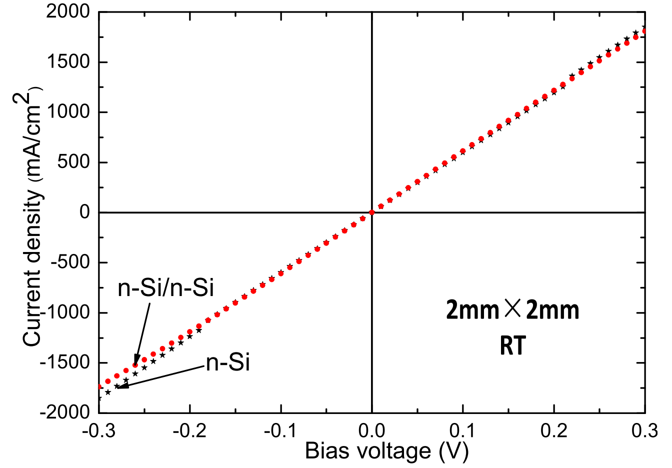

FIG. 2. *I-V* characteristics of *n*-Si/*n*-Si junction measured at room temperature.

Figure 2 compares the *I-V* characteristics of the *n*-Si/*n*-Si junctions with those of *n*-Si substrates with contacts on both surfaces, measured at room temperature. The *I-V* characteristics of both samples show excellent linearity and the discrepancy between their *I-V* characteristics is small. Similar results were recently reported for n-Si/n-GaAs junctions.[19,20] From a least square fitting, the resistances of the *n*-Si/*n*-Si junctions and the *n*-Si substrates were determined to be 0.17 and 0.16 $\Omega \cdot cm^2$, respectively. The difference may be due to the differences in sample thicknesses and in the resistance across the bonding interfaces in the *n*-Si/*n*-Si junctions. These results indicate that the influence of a potential barrier across the bonded interface on the conductive properties, if any, should be small in comparison with that of the sum of the contact resistance and the resistance in the *n*-Si substrates.

Figure 3(a) shows the *I-V* characteristics of the *p*-Si/*n*-Si junction, measured at room temperature. As is seen in the "as-measured" curves, the current for forward-bias voltages higher than 0.5 V is almost proportional to the bias voltages, which suggests that the conduction properties in this voltage region are dominated by parasitic resistance. We estimated the parasitic resistance from the slope of the curve and obtained the "treated" *I-V* characteristics by subtracting its contribution from the "as-measured" curve. The intrinsic electrical properties, or the properties at the bonding interfaces, are assumed to appear in the treated curve. We also calculated the *I-V* characteristics in the framework of a Schockley model using the reported dependence of the life time and mobility of the minority carriers on the concentration of the majority carriers.[21,22] The obtained *I-V* characteristics are labeled "modeled."

Both the as-measured and treated *I-V* characteristics reveal rectifying properties similar to those in conventional pn junctions. For both curves, the turn-on voltage is the

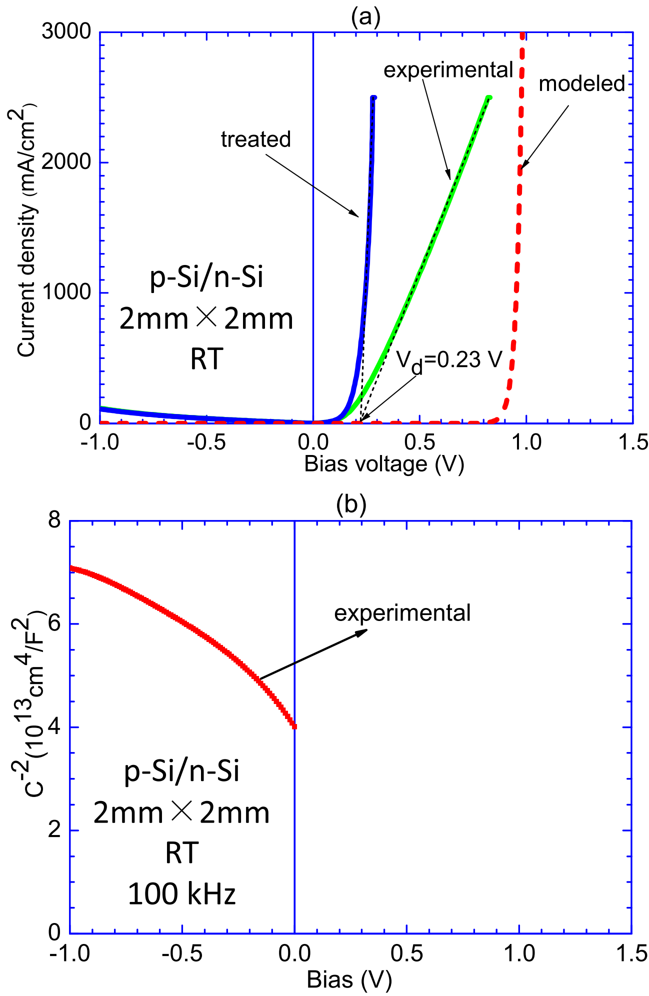

FIG. 3. (a) *I-V* and (b) *C-V* characteristics of *p*-Si/*n*-Si junctions measured at room temperature.

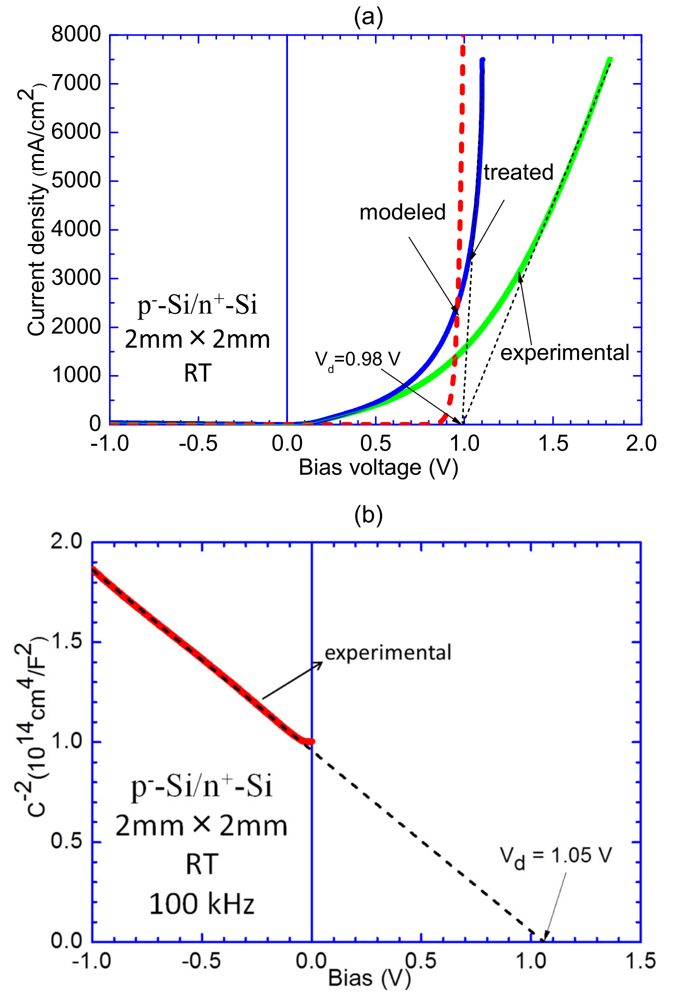

FIG. 4. (a) *I-V* and (b) *C-V* characteristics of p^{-}-Si/n^{+}-Si junctions measured at room temperature.

same, ~0.23 V, which is surprisingly small compared to that of the modeled curve (0.95 V). The currents for reverse-bias voltages in the as-measured and treated *I-V* characteristics are larger than that of the modeled characteristics. The $1/C^2$-V characteristics of a *p*-Si/*n*-Si junction measured at 100 kHz are shown in Fig. 3(b), in which a marked warp is observed.

Figure 4(a) shows the as-measured, treated, and modeled curves of the *I-V* characteristics of the p^{-}-Si/n^{+}-Si junction, measured at room temperature. The as-measured and treated curves exhibit rectifying properties. In addition, the turn-on voltage is ~0.98 V, which is close to that for the modeled curve (0.93 V). Figure 4(b) shows the $1/C^2$-V characteristics of the p^{-}-Si/n^{+}-Si junction measured at 100 kHz, the result is a straight line. Using its slope, the concentration of ionized acceptors in the p^{-}-Si substrate was estimated to be $1.5 \times 10^{17}\,\mathrm{cm}^{-3}$, which is close to that obtained from Hall measurement ($2.4 \times 10^{17}\,\mathrm{cm}^{-3}$). From the capacitance value, we also estimated the thickness of the depletion layer and obtained a value of approximately 100 nm at zero-bias voltage. The diffusion potential was found to be ~1.05 V by linearly extrapolating $1/C^2$ to zero.

The *I-V* characteristics of *p*-Si/*n*-Si and p^{-}-Si/n^{+}-Si junctions measured at various temperatures are shown in Figs. 5(a) and 5(b). Note that the magnitude of the current increases in both *p*-Si/*n*-Si and p^{-}-Si/n^{+}-Si junctions with increasing depth of the reverse bias. The magnitude of the current also increases with increasing temperature. We also find that the slope of the current for reverse-bias voltages between 0.3 and 0.75 V in the *p*-Si/*n*-Si junctions is not sensitive to the ambient temperature. The slope in the p^{-}-Si/n^{+}-Si junctions, in contrast, decreases as the ambient temperature increases.

III. DISCUSSION

Noting that the characteristic X-ray signals in EDS measurements are generated in a region with a depth of a few micrometers, the scattering characteristics of the atomic ratio of oxygen among the a1, a2, a3, a4, and a5 areas might be attributable to possible fluctuations in the thickness of the native oxides formed on the side of samples exposed to air by dicing. This suggests that there is no oxide layer at the Si/Si interface, which is consistent the parasitic resistance's being larger than that across the interfaces in the *n*-Si/*n*-Si junctions (Fig. 2). The result is in large contrast to that for conventional wafer bonding, where the resistance across the bonding interfaces has been reported to be larger than their

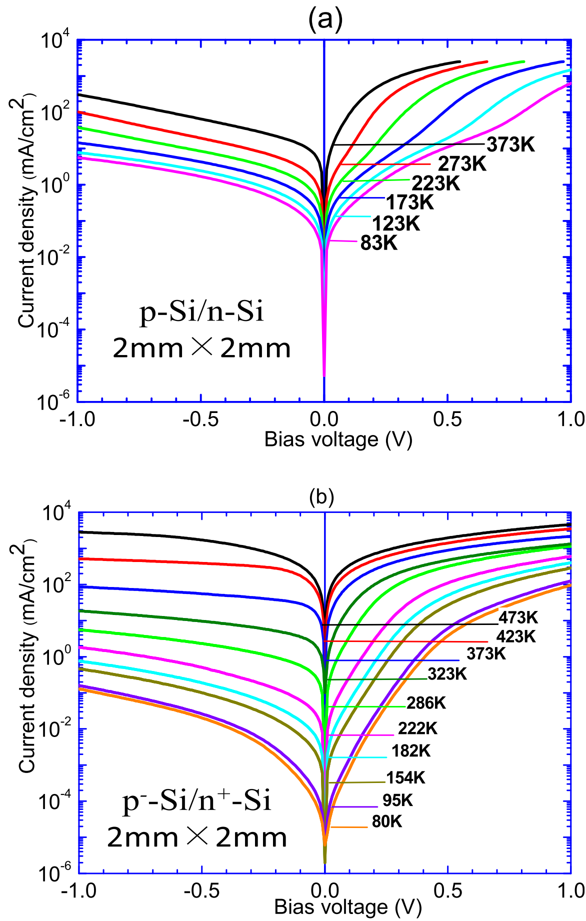

FIG. 5. *I-V* characteristics of (a) *p*-Si/*n*-Si and (b) p^--Si/n^+-Si junctions measured at various temperatures.

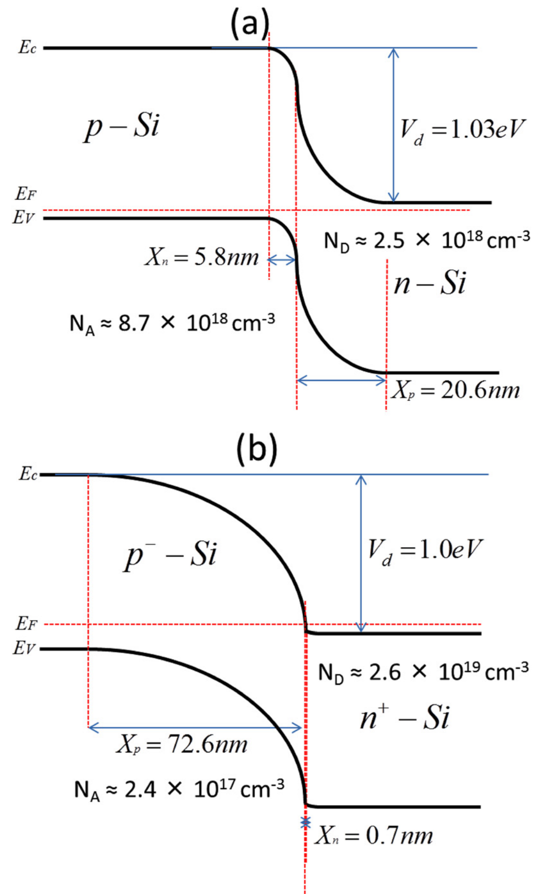

FIG. 6. Schematic energy-band diagram of (a) *p*-Si/*n*-Si and (b) p^--Si/n^+-Si junctions.

parasitic resistance,[23] presumably due to residual oxide layers formed at the interfaces achieved.[6,8]

Figures 6(a) and 6(b) show energy-band diagrams of the *p*-Si/*n*-Si and p^--Si/n^+-Si junctions, respectively, at zero-bias voltage and at room temperature. These diagrams are based on the carrier concentrations of the respective substrates shown in Table I. Note that these diagrams stem from the assumption that there are no additional charges located at the interfaces. The diffusion potentials are found to be 1.03 and 1.0 V for the *p*-Si/*n*-Si and p^--Si/n^+-Si junctions, respectively. The total depletion layer thicknesses are estimated to be 26.4 and 73.3 nm for the *p*-Si/*n*-Si and p^--Si/n^+-Si junctions, respectively.

For the *p*-Si/*n*-Si junctions, we observed a large discrepancy between the diffusion potential (1.03 V) and the turn-on voltage (0.23 V) in the *I-V* characteristics. Similar discrepancies reported for *p*-GaAs/*n*-GaN and *p*-SiC/*n*-GaN heterojunctions fabricated by wafer fusion.[24–26] In addition, a warp in the $1/C^2$-V characteristics, which we observed for the *p*-Si/*n*-Si junctions, has also been reported for *n*-Ge/*p*-Si diodes.[27] Such discrepancies between the turn-on voltages, the expected diffusion potential, and warps appearing in the $1/C^2$-V characteristics have been explained[25–28] by assuming that carriers tunnel through the possibly formed interface states and some of the carriers become trapped at such states so that the electrical charges are placed at the interfaces.

In the present work, the Ar plasma irradiation in the SAB process is assumed to induce the interface states. Such interface states or traps should be distributed in the 9 nm thick transition layer [Fig. 1(a)], which was likely to be made due to the Ar plasma irradiation. Although the interface states are likely formed in *p*-Si/*n*-Si and p^--Si/n^+-Si junctions during the Ar plasma irradiation, we observed marked discrepancies neither between the turn-on voltage and the diffusion potential nor between it and the warps in the $1/C^2$-V characteristics for the p^--Si/n^+-Si junctions.

The difference mentioned above between the *p*-Si/*n*-Si and p^--Si/n^+-Si junctions might be related to their depletion layer thicknesses: Given that the total thickness of the depletion layer in the *p*-Si/*n*-Si junctions, 26.4 nm at zero-bias voltage, is comparatively close to (approximately only three times as large as) the thickness of the transition layers, the characteristics measured for the *p*-Si/*n*-Si junctions are assumed to be more strongly influenced by the properties in the bonding interfaces. In the p^--Si/n^+-Si junctions, in contrast, the depletion layers in the p^--Si substrates, which are 72.6-nm thick at the zero bias voltage, are much thicker than the transition layers, while the depletion layers in the n^+-Si substrates, 0.7-nm thick at the zero bias voltage, are much thinner. It is assumed, consequently, that the impact of the properties of the bonding interfaces on the turn-on voltage and the $1/C^2$-V characteristics in the p^--Si/n^+-Si junctions is smaller than in the *p*-Si/*n*-Si junctions.

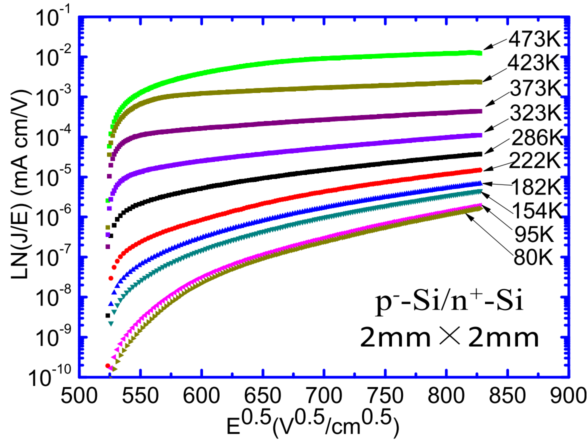

FIG. 7. Measured reverse-bias current density divided by electric field vs square root of electric field for p^--Si/n^+-Si junctions at temperatures ranging from 473 to 80 K.

The electrical properties in the *n*-Si/*n*-Si junctions are also assumed to be influenced by the states at the bonding interfaces. The results of measurements of *I-V* characteristics, however, suggest that their impact on the conductive properties is comparatively small in the *n*-Si/*n*-Si junctions.

In the *I-V* characteristics of the *p*-Si/*n*-Si junctions, the fact that the slope of the current for reverse-bias voltages between 0.3 and 0.75 V in the semi-log scale is not sensitive to the ambient temperature [Fig. 5(a)] suggests that the tunneling process dominates the transport of carriers across the interfaces. A numerical analysis has shown that the features of the *I-V* characteristics for reverse-bias voltages can be explained by the view of the trap-assisted tunneling through 0.2 eV traps,[14] which are assumed to be related to the interface states.

Figure 7 shows the relationships between the ratio of the current density (*J*) to the maximum electric field (*E*) in the junctions and the square root of *E* of the p^--Si/n^+-Si junctions, which were extracted from their *I-V* characteristics for reverse-bias voltages. We find that the relationship between ln(*J*/*E*) and $\sqrt{E}$ is close to a straight line for *E* between 360 and 685 kV/cm ($\sqrt{E}$ between 600 and 828 $V^{0.5}/cm^{0.5}$) at each temperature. The relationship between the slope of the lines ($\partial \ln(J/E)/\partial\sqrt{E}$) obtained for the above electric field range and the inverse of temperature is shown in Fig. 8. Also shown is a straight line, which corresponds to

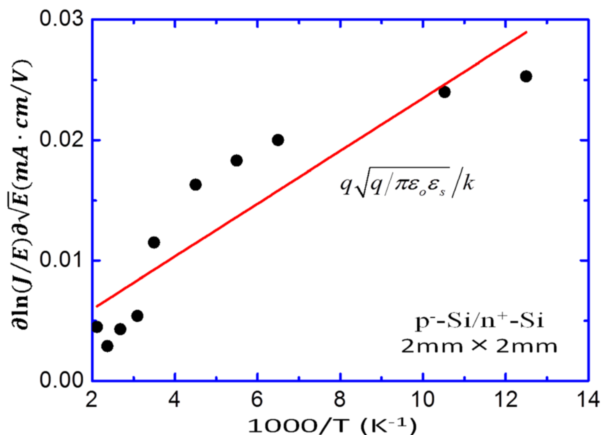

FIG. 8. Slope of the curves shown in Fig. 7 for the p^--Si/n^+-Si junctions.

$$\partial \ln(J/E)/\partial\sqrt{E} = q(q/\pi\varepsilon_o\varepsilon_s)^{1/2}/k_BT, \quad (1)$$

where ε_o and ε_s are vacuum permittivity and the dielectric constant of Si, respectively. Each data point in this figure is placed along this line, which suggests that the transport properties of carriers in the reverse-biased p^--Si/n^+-Si junctions can be semi-quantitatively explained using the Frenkel-Poole model,[29,30] as in the case of metalorganic chemical vapor deposition (MOCVD)-grown InGaN *pn* junctions.[31] We actually confirmed (not shown) that the results of analyses using other models, such as the generation-recombination model,[32] band--to-band tunneling model,[33] field-emission tunneling model,[34] and trap-assisted tunneling model[14] are not in agreement with the measurements for the p^--Si/n^+-Si junctions.

Similar to the difference in the turn-on voltage and $1/C^2$-*V* characteristics, the difference in the likely mechanisms that dominate the carrier transport for reverse-bias voltages between the *p*-Si/*n*-Si and the p^--Si/n^+-Si junctions might be related to the depletion layer thickness in the two junctions.

IV. CONCLUSION

We investigated the electrical properties of *n*-Si/*n*-Si, *p*-Si/*n*-Si, and p^--Si/n^+-Si junctions fabricated by using SAB. TEM observations of the vicinities of the bonding interfaces of the *n*-Si/*n*-Si junctions, indicated a transition layer is likely to be formed by the Ar plasma irradiation in the surface activation process. In EDS measurements, we observed no evidence of oxide layers at the bonding interfaces. The measurements of *I-V* and $1/C^2$-*V* characteristics of the *p*-Si/*n*-Si and p^--Si/n^+-Si junctions revealed that the states at the bonding interfaces, likely to be formed in the transition layer during the surface activation process, had a more marked impact on the electrical properties in the *p*-Si/*n*-Si junctions. The carrier transport properties for the reverse-biased *p*-Si/*n*-Si and p^--Si/n^+-Si junctions can be explained by using the trap-assisted tunneling model and the Frenkel-Poole model, respectively. The difference in the electrical properties between the *p*-Si/*n*-Si and p^--Si/n^+-Si junctions might be related to their depletion layer thicknesses. Furthermore, the impact of the interface states on the electrical properties of the *n*-Si/*n*-Si junctions was found to be small.

ACKNOWLEDGMENTS

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