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2016 Jpn. J. Appl. Phys. 55 068002

(http://iopscience.iop.org/1347-4065/55/6/068002)

Japanese Journal of Applied Physics **55**, 068002 (2016)
http://doi.org/10.7567/JJAP.55.068002

BRIEF NOTE

Effects of annealing on the electrical characteristics of GaAs/GaAs junctions by surface-activated bonding

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Received January 14, 2016; accepted March 16, 2016; published online May 17, 2016

The electrical properties of GaAs/GaAs junctions fabricated by surface-activated bonding (SAB) and annealing were examined on the basis of the charge neutral level model. The potential barrier height, the density of interface states, and the charge neutral level at GaAs/GaAs interfaces were estimated from the measured dependences of the electrical conductance of n-GaAs/n-GaAs and p-GaAs/p-GaAs junctions on ambient temperature. The barrier height and the density of interface states were lowered by increasing the annealing temperature to 400 °C, which suggested that the damage introduced during the SAB process was partly reduced. © 2016 The Japan Society of Applied Physics

Wafer bonding technologies are useful for fabricating heterostructures made of dissimilar semiconductor materials with different crystal structures, lattice constants, and thermal expansion coefficients, which cannot be easily made by means of conventional crystal growth technologies.[1] Among the various wafer bonding methods, surface-activated bonding (SAB),[2–5] in which samples are bonded to each other without heating after their bonding surfaces are activated using the fast atom beam (FAB) of noble gas species such as Ar, has been successfully applied to fabricating a variety of heterojunctions such as Si/GaAs,[4,6,7] Si/InP,[5] Si/GaN,[8] and Si/SiC[9] systems as well as Si/Si[10,11] and GaAs/GaAs[12] homojunctions. We previously applied SAB to fabricating III–V-on-Si hybrid tandem solar cells with GaAs/Si bonding interfaces so that a high conversion efficiency of ≈26% was demonstrated.[13] We also fabricated SiC/Si heterojunction bipolar transistors with SAB-based SiC emitter/Si base junctions and observed current gains.[14]

GaAs/GaAs homojunctions were also fabricated by direct wafer bonding.[15,16] Their current–voltage (I–V) characteristics were sensitive to the prebonding treatments of GaAs surfaces and temperatures of the postbonding annealing. The change in the I–V characteristics was discussed in relation to the variation of the amorphous-like intermediate layers at the bonding interfaces.

It was reported that amorphous-like intermediate layers were also formed at the SAB-based bonding interfaces due to the FAB and they were recrystallized when the interfaces were annealed.[3] Furthermore, it was pointed out that the resistance across the bonding interfaces in GaAs/GaAs junctions was approximately correlated with the thickness of the amorphous-like layers by characterizing junctions fabricated using different species for the FAB.[12] It is assumed, consequently, that the interface states should be formed at the bonding interfaces and their density (D_{it}) might be varied due to the annealing. Actually, we extracted D_{it} as well as the charge neutral level (CNL) at the annealed Si/Si interfaces using a framework based on the CNL model and discussed their dependences on annealing temperature.[11] In this work, we examined the properties of annealed GaAs/GaAs junctions by a similar process.

We prepared n-GaAs and p-GaAs epitaxially grown substrates, which were made of n-GaAs (donor concentration $N_D \sim 1.6 \times 10^{16}\,cm^{-3}$, 50 nm)/n$^+$-GaAs ($N_D \sim 2.0 \times 10^{19}\,cm^{-3}$, 50 nm) bilayers on n-GaAs (100) substrates and p-GaAs (acceptor concentration $N_A \sim 2.5 \times 10^{17}\,cm^{-3}$, 50 nm)/p$^+$-GaAs ($N_A \sim 1 \times 10^{19}\,cm^{-3}$, 50 nm) bilayers on p-GaAs (100) substrates, respectively. Ohmic contacts on their backsides were formed by evaporating AuGe/Ni/Au and AuZn/Ti/Au, respectively, and annealing at 400 °C for 1 min in nitrogen ambient. Then, n-GaAs/n-GaAs and p-GaAs/p-GaAs junctions were fabricated by SAB without heating. We annealed the interfaces at 200 °C for 5 min, 300 °C for 5 min, and 400 °C for 1 min, respectively.

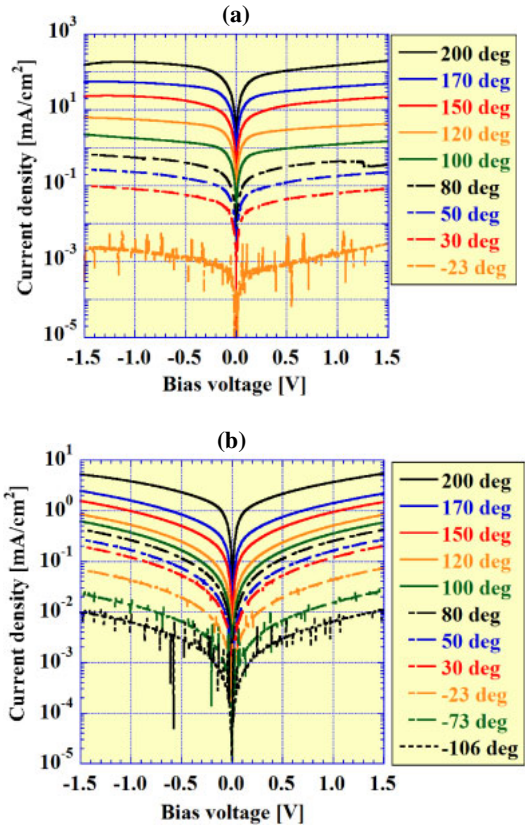

Fig. 1. (Color online) I–V characteristics at 300-°C-annealed (a) n-GaAs/n-GaAs and (b) p-GaAs/p-GaAs bonding interfaces. The ambient temperatures for the respective curves are also shown.

We measured the I–V characteristics of the n-GaAs/n-GaAs junctions at an ambient temperature T between −23 and 200 °C. Those of the p-GaAs/p-GaAs junctions were measured at T between −106 and 200 °C. The I–V characteristics of the n-GaAs/n-GaAs and p-GaAs/p-GaAs junctions annealed at 300 °C are shown in Figs. 1(a) and 1(b), respectively. As typically shown in these figures, the current increased (the interface resistance decreased) as the ambient

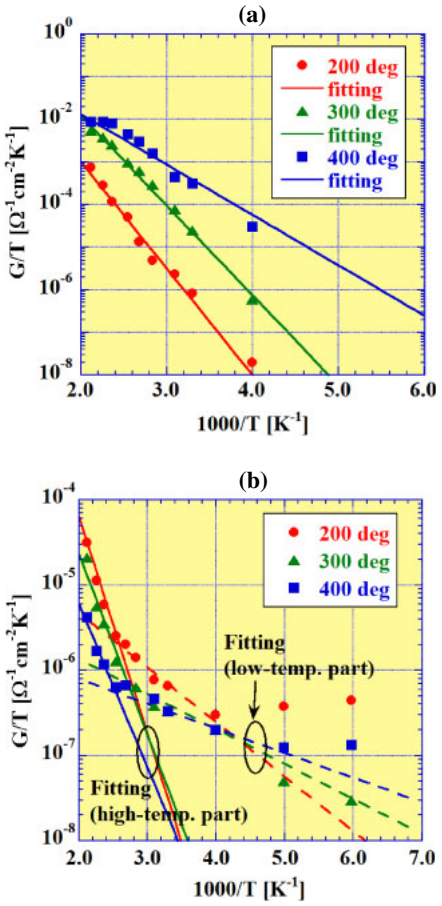

Fig. 2. (Color online) Relationships between the conductance at 0 V divided by the ambient temperature, G/T, and $1/T$ for (a) n-GaAs/n-GaAs and (b) p-GaAs/p-GaAs junctions. Results of fitting to straight lines are also shown. High- and low-ambient-temperature parts of the results for p-GaAs/p-GaAs junctions were separately fitted to lines.

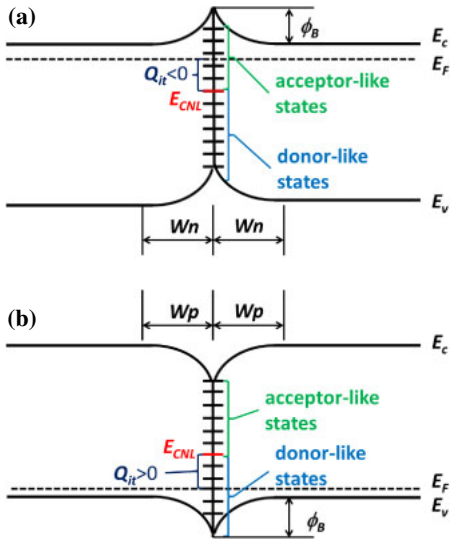

Fig. 3. (Color online) Schematic band diagrams of (a) n-GaAs/n-GaAs and (b) p-GaAs/p-GaAs junctions.

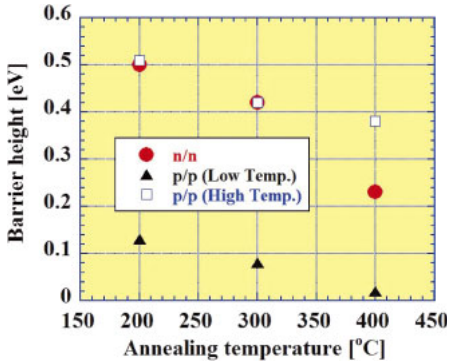

Fig. 4. (Color online) The relationships between the extracted potential barrier heights and the annealing temperature. Two barrier heights, which were estimated from the data for the low- and high-ambient temperatures, are shown for the p-GaAs/p-GaAs junctions.

temperature increased. We observed slight unsymmetrical properties in the I–V curves, which might be attributable to the unideal characteristics in contacts on the back sides of GaAs substrates. Their impacts on the analysis in the present work are assumed to be negligible. The conductance at a bias voltage of 0 V, G, was extracted from each I–V curve. The relationships between the conductance divided by the ambient temperature, G/T, and $1/T$ are shown in Figs. 2(a) and 2(b) for the n-GaAs/n-GaAs and p-GaAs/p-GaAs junctions, respectively. We found that G/T increased as $1/T$ decreased.

Hereafter, the following assumptions were employed for analyzing the experimental results. (i) D_{it} is independent of the energy of the states across the bandgap. (ii) Both E_{CNL}, the energy of CNL measured from the valence band edge of GaAs, and D_{it} are insensitive to the concentration of dopants and the polarity of substrates. They depend on the conditions of the SAB and post bonding processes. (iii) The potential barrier $q\phi_B$ with q as the elementary charge is formed at the bonding interface so as to compensate for the interface charges, as shown in Figs. 3(a) and 3(b) for the n-GaAs/n-GaAs and p-GaAs/p-GaAs junctions, respectively. In these figures, W_n and W_p are the depletion layer thicknesses of n-GaAs and p-GaAs layers, respectively. (iv) The transport properties of carriers across the bonding interfaces are described by the thermionic emission model.

On the basis of these assumptions, we fitted each relationship between $\ln(G/T)$ and $1/T$ for the n-GaAs/n-GaAs junction to a straight line so that $q\phi_B$ at each annealing temperature was estimated. The results of fitting are shown in Fig. 2(a). Given that each relationship for the p-GaAs/p-GaAs junctions was separated into a high-temperature part with a large slope and a low-temperature part with a small slope, two barrier heights were obtained by fitting the respective parts to straight lines as shown in Fig. 2(b). The obtained barrier heights, which are summarized in Fig. 4, decreased as the annealing temperature increased. This result is in good contrast to that for Si/Si junctions, which showed that the barrer height of the n-Si/n-Si (p-Si/p-Si) junctions increased as the annealing temperature increased to 600 (400) °C but decreased as the annealing temperature was further increased.[11)]

The higher concentration of dopants in the p-GaAs layer ($N_A \sim 2.5 \times 10^{17}\,cm^{-3}$) in comparison with those in the n-GaAs layer indicates that the depletion layer of the p-GaAs layer is narrower [$W_p < W_n$ in Figs. 3(a) and 3(b)] so that the features of tunneling across the potential barrier are more apparent in the transport characteristics in the p-GaAs/p-GaAs junction. This scheme suggests that the smaller

Table I. E_{CNL} and D_{it} at each annealing temperature.

	200 °C	300 °C	400 °C
E_{CNL} (eV)	0.79	0.82	1.00
D_{it} ($cm^{-2}eV^{-1}$)	2.0×10^{13}	7.8×10^{12}	4.3×10^{12}

barrier heights achieved for the p-GaAs/p-GaAs junctions (0.02–0.13 eV) might be the contribution of such tunneling process of holes. Consequently, we assumed that the larger barrier heights (0.38–0.51 eV) reflect the intrinsic characteristics of p-GaAs/p-GaAs interfaces.

We estimated E_{CNL} and D_{it} by analyzing the barrier heights of junctions on the basis of the above-mentioned assumptions. The results are given in Table I. We found that D_{it} decreased as the annealing temperature increased (from $\approx 2.0 \times 10^{13}\,cm^{-2}\,eV^{-1}$ at 200 °C to $\approx 4.3 \times 10^{12}\,cm^{-2}\,eV^{-1}$ at 400 °C). E_{CNL} (0.79–1.00 eV) was found to be higher than that in the literature (0.5 eV in Ref. 17).

These features were in agreement with the observation for Si/Si junctions. The high E_{CNL} in comparison with that in a previous report might be related to the possible formation of donor-like states due to the Ar beam irradiation.[18] The decreases in $q\phi_B$ and D_{it} due to the annealing, which mean that the damage caused by the Ar beam irradiation in the SAB process is reduced, are useful for exploring the possibility of applying SAB to the III–V-material-based device process.

In conclusion, we fabricated n-GaAs/n-GaAs and p-GaAs/p-GaAs junctions by surface-activated bonding and measured their current–voltage characteristics after annealing. We estimated the heights of the potential barriers, the charge neutral level, E_{CNL}, and the density of interface states, D_{it}, at GaAs/GaAs interfaces. The decrease in D_{it} due to the annealing, which is in agreement with the results for Si/Si junctions, might play a crucial role in fabricating SAB-based devices.

Acknowledgments This work was supported in part by the "Research and Development of ultra-high efficiency and low-cost III–V compound semiconductor solar cell modules (High efficiency and low-cost III–V/Si tandem)" project of New Energy and Industrial Technology Development Organization (NEDO). The authors are grateful to M. Morimoto for his advice in data analysis.

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