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Electrical properties of GaAs//indium tin oxide/Si junctions for III–V-on-Si hybrid multijunction cells

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The electrical properties of GaAs//indium tin oxide (ITO)/Si junctions fabricated by surface-activated bonding (SAB) are investigated with emphasis on their dependence on the temperature of postbonding annealing. The current–voltage (*I–V*) characteristics of n^+-GaAs//ITO/p^+-Si and n^+-GaAs//ITO/n^+-Si junctions without annealing are linear. Those of p^+-GaAs//ITO/p^+-Si and p^+-GaAs//ITO/n^+-Si junctions without annealing are nonlinear. Although the interface resistance of all the junctions increases with increasing annealing temperature, the resistances of the respective junctions after the annealing at 400 °C are still smaller than the series resistance of the actual SAB-based InGaP/GaAs//Si hybrid triple-junction cells (~4 Ω cm^2). The n^+-GaAs//ITO/n^+-Si junction reveals the lowest resistance among the investigated junctions after annealing. These results demonstrate that GaAs//ITO/Si junctions with an ITO intermediate layer could be effective for reducing series resistance in hybrid multijunction cells.

1. Introduction

III–V/Si-based multijunction solar cells have been promising as next-generation solar cells since they can provide high efficiency, and low cost in comparison with conventional Si and III–V multijunction cells.[1–3] In case of the epitaxially grown III–V-on-Si cells, however, a high density of interface states are introduced at the III–V/Si interfaces because of a large mismatch in the crystal lattice constants and thermal expansion coefficients.[4,5] Instead of the epitaxial growth, surface-activated bonding (SAB) methods have been applied to fabricate macroscopic defect-free III–V/Si hetero-interfaces.[6,7] In the SAB,[8–11] the surfaces of the substrates to be bonded are irradiated by the fast atom beam (FAB) of Ar. Then the native oxide layers on the surface of the substrates are removed, or the surfaces are activated. In the next step, the substrates are weighted at room temperature. Using SAB, dissimilar semiconductor substrates with different lattice constants and thermal expansion coefficients can be directly bonded to each other without heating. Previously, SAB-based InGaP/Si,[12] GaN/Si,[13] and InGaP/GaAs/Si[14,15] multijunction solar cells were reported by the present authors.

The bonding interfaces with lower interface resistances are strongly required so as to achieve better performances of hybrid multijunction cells. The electrical conductivity of the bonding interface was improved by increasing the doping concentration of the bonding semiconductor.[16] In addition, it was reported that the interface resistance of SAB-based junctions was decreased by annealing at low temperatures since the damages introduced at the bonding interface due to the FAB irradiation were partially eliminated.[17–20] The interface resistance of SAB-based GaAs/Si junctions[18] is, however, still much larger than that of the lattice-matched III–V/IV interface formed by epitaxial growth.[21] Also, we previously reported that the interface resistance in the actual hybrid InGaP/GaAs/Si triple-junctions cells was estimated to be ~4 Ω cm^2,[15] which was ~30 times larger than the interface resistance obtained for the bonding interface made of heavily doped substrates or epitaxially grown layers.[18]

Indium tin oxide (ITO) is widely known as an n-type degenerate semiconductor with a band gap of around 3.5 to 4.3 eV.[22,23] The electrical and optical properties of ITO are very attractive for optoelectronic devices such as solar cells, light-emitting diodes, laser diodes, and photodetectors because of its relatively low electrical resistivity (~10^{-4} Ω cm) and high transmittance in the visible range of the solar spectrum.[24–26] We successfully bonded an ITO film deposited on a Si substrate to another Si substrate using SAB[27] and fabricated InGaP/GaAs/ITO/Si hybrid triple-junction cells with ITO intermediate layers.[28]

The understanding of the electrical properties and structures of the heavily doped GaAs//ITO bonding interfaces is important in designing hybrid multijunction cells with ITO intermediate layers. In this work, we investigated the annealing effects on p^+-GaAs//ITO/p^+-Si, n^+-GaAs//ITO/p^+-Si, n^+-GaAs//ITO/n^+-Si, and p^+-GaAs//ITO/n^+-Si junctions fabricated by the SAB method by measuring current–voltage (*I–V*) characteristics. Also, we investigated the band structures of n^+-GaAs/ITO and p^+-GaAs/ITO bonding interfaces by estimating the barrier heights, which were calculated from the *I–V* characteristics over the wide temperature range of p-GaAs//ITO/n^+-Si and n-GaAs//ITO/n^+-Si junctions fabricated by the SAB method.

2. Experimental methods

We used two types of Si substrates and four types of GaAs epitaxial layers on GaAs substrates for SAB experiments. Their carrier concentrations are shown in Table I. Hall measurements at room temperature revealed that the resistivity and carrier concentrations of the p^+-Si and n^+-Si substrates were 0.003 Ω cm and (N_A =) 2.64×10^{19} cm^{-3}, and 0.002 Ω cm and (N_D =) 2.64×10^{19} cm^{-3} for the p^+-Si and n^+-Si substrates, respectively.

100 nm ITO films were deposited on Si substrates and glass plates by reactive plasma deposition.[29] The Si substrates were not irradiated by Ar FAB before depositing. The surface of the ITO films deposited on a Si substrate was observed by atomic force microscopy (AFM) using Shimadzu SPM-9600. The transmittance and reflectance of ITO films deposited on a glass plate were measured using JASCO V-550. We measured the resistivities of the ITO films on glass plates without and with Ar irradiation by the circular

Table I. Carrier concentration and thickness of substrates.

	Type	Carrier concentration (cm^{-3})	Thickness (μm)
p^+-Si	(100) substrate	2.64×10^{19}	525
n^+-Si	(100) substrate	2.64×10^{19}	525
n^+-GaAs	Epitaxial layer	$\sim 1 \times 10^{19}$	0.4
	(100) substrate	$\sim 1 \times 10^{18}$	340
p^+-GaAs	Epitaxial layer	$\sim 1 \times 10^{19}$	0.4
	(100) substrate	$\sim 1 \times 10^{18}$	340
n-GaAs	Epitaxial layer	$\sim 1 \times 10^{17}$	0.35
	Epitaxial layer	$\sim 1 \times 10^{19}$	0.05
	(100) substrate	$\sim 1 \times 10^{18}$	340
p-GaAs	Epitaxial layer	$\sim 1 \times 10^{17}$	0.35
	Epitaxial layer	$\sim 1 \times 10^{19}$	0.05
	(100) substrate	$\sim 1 \times 10^{18}$	340

transmission line model (CTLM) method without and with annealing at 200, 300, and 400 °C for 300 s in N_2 ambient. Note that all the CTLM samples were annealed at 120 °C during the sample preparation.

Before bonding, ohmic contacts were formed by evaporating Al/Ni/Au, Ti/Au, AuZn/Ti/Au, and AuGe/Ni/Au multilayers on the back side surfaces of p^+-Si, n^+-Si, p-GaAs, and n-GaAs substrates, respectively. The GaAs substrates were annealed at 400 °C for 60 s in N_2 ambient after the evaporation. Then we fabricated p^+-GaAs//ITO/p^+-Si (Sample A), n^+-GaAs//ITO/p^+-Si (Sample B), n^+-GaAs//ITO/n^+-Si (Sample C), p^+-GaAs//ITO/n^+-Si (Sample D), p-GaAs//ITO/n^+-Si (Sample E), and n-GaAs//ITO/n^+-Si (Sample F) junctions by SAB. The conditions of bonding were the same as those used in a previous work.[11] The GaAs//ITO/Si junctions made of the heavily doped GaAs epitaxial layers were annealed at 100, 200, 300, and 400 °C for 300 s in N_2 ambient. All the samples were diced into $2 \times 2\,mm^2$ pieces. Their *I–V* characteristics were measured at room temperature using Agilent B2902A. In addition, *I–V* measurements of Samples E and F were carried out at temperatures between 90 and 475 K. The bonding interfaces of the GaAs//ITO/Si junctions were investigated by field emission-scanning electron microscopy (FE-SEM) using JEOL JSM6500F.

3. Results

3.1 Fundamental properties of ITO films

Figure 1 shows an AFM image of the surface of the ITO film deposited on Si substrates. The surface roughness of ITO films was found to be ≈0.4 nm, which was sufficiently small for the films to be firmly bonded to GaAs substrates. The transmittance *T* and the reflectance *R* of ITO films deposited on glass plates are shown in Fig. 2(a). The absorption coefficient α is calculated from the transmittance and reflectance using the following equation:[30]

$$\alpha = \frac{1}{d} \ln \frac{2TR^2}{\sqrt{(1-R)^4 + 4T^2R^2} - (1-R)^2}, \quad (1)$$

where *d* is the thickness of ITO films. α obtained for ITO films without and with Ar irradiation is shown in Fig. 2(b). Figure 2(c) shows the dependence of $(\alpha h\nu)^2$, where $h\nu$ is photon energy, on $h\nu$. From this figure, the optical band gap

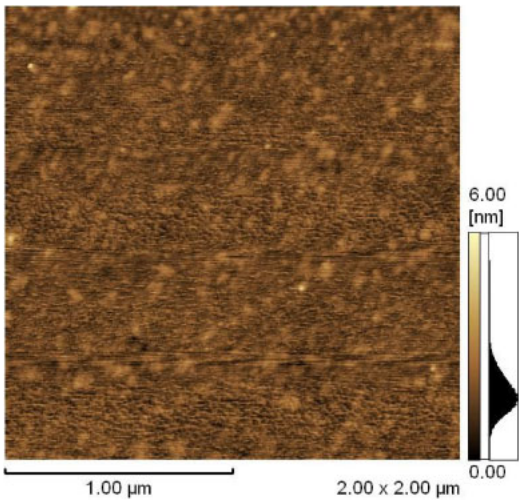

Fig. 1. (Color online) AFM image of surface of ITO film on Si substrate.

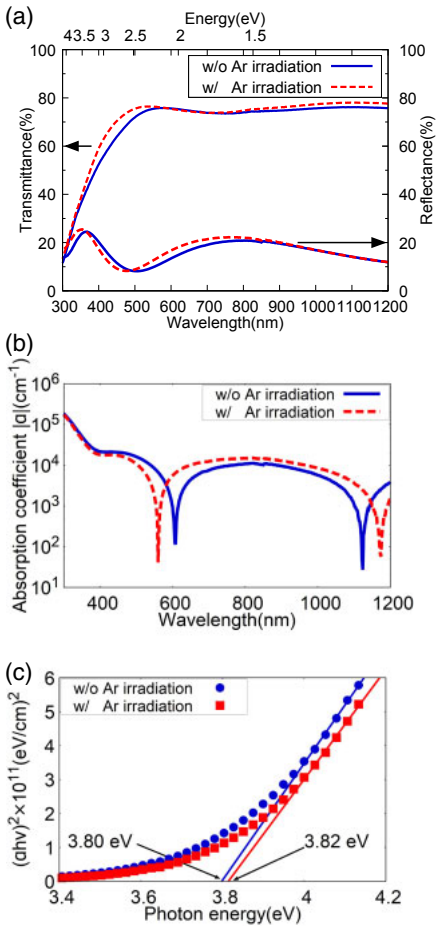

Fig. 2. (Color online) (a) Transmittance and reflectance of ITO film on glass plates, (b) absorption coefficient of ITO films calculated from transmittance and reflectance of respective samples, and (c) optical band gap energy of ITO films without and with Ar irradiation.

energy of ITO films without and with Ar irradiation was found to be 3.80 and 3.82 eV, respectively.

The concentrations of electrons in 100 nm ITO films without and with Ar irradiation were found to be 1.08×10^{21} and $1.22 \times 10^{21}\,cm^{-3}$, respectively, by Hall measurements. Figure 3 shows the relationship between the resistivity of the ITO film on a glass plate and annealing temperature. The

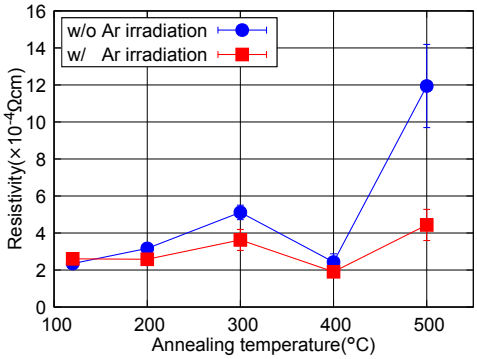

Fig. 3. (Color online) Resistance of ITO films without and with Ar irradiation as a function of annealing temperature. The error bars represent the 1σ standard deviation of the mean.

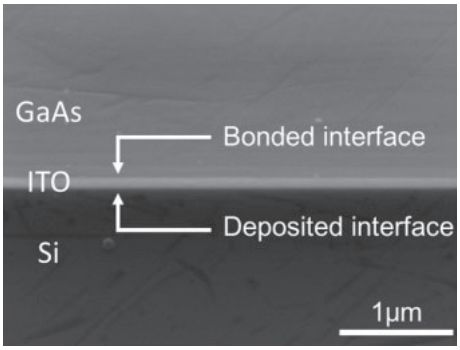

Fig. 4. Cross-sectional FE-SEM image of GaAs//ITO/Si interface.

resistivity of the ITO film without Ar irradiation was estimated to be 2.35×10^{-4}, 3.17×10^{-4}, 5.12×10^{-4}, 2.43×10^{-4}, and $1.19 \times 10^{-3}\,\Omega\,\mathrm{cm}$ without and with annealing at 200, 300, 400, and 500 °C, respectively. The resistivity of the ITO film after Ar irradiation was estimated to be 2.60×10^{-4}, 2.58×10^{-4}, 3.62×10^{-4}, 1.90×10^{-4}, and $4.44 \times 10^{-4}\,\Omega\,\mathrm{cm}$ without and with annealing at 200, 300, 400, and 500 °C, respectively. These results suggests that the influence of Ar irradiation on ITO is negligible.

3.2 Electrical properties of GaAs//ITO/Si junctions

Figure 4 shows an FE-SEM image of the cross section of the GaAs//ITO/Si interface without annealing. As shown in Fig. 4, a 100 nm ITO layer was observed. There were no structural defects and voids observed along the bonded interface.

Figure 5 shows the *I–V* characteristics of Samples A, B, C, and D measured between −0.1 and 0.1 V at room temperature. We found that the *I–V* characteristics of Samples B and C are linear. In contrast, the *I–V* characteristics of Samples A and D are nonlinear. The interface resistances of Samples A, B, C, and D were estimated to be 0.208, 0.042, 0.079, and $0.172\,\Omega\,\mathrm{cm}^2$, respectively, by the least-square fitting between −0.01 and 0.01 V.

The room-temperature *I–V* characteristics of Samples A, B, C, and D after annealing are shown in Figs. 6(a)–6(d), respectively. After annealing at higher temperatures, the nonlinear feature was more marked in the *I–V* characteristics of these GaAs//ITO/Si junctions. We estimated the interface resistance from each curve by least-square fitting between −0.01 and 0.01 V. The relationships between the obtained interface resistance and the annealing temperature are shown in Fig. 6(e). We found that the resistances of all the samples increased with increasing annealing temperature. It was notable that the resistance of n^+-GaAs//ITO junctions was smaller than that of p^+-GaAs//ITO junctions. Specifically, Sample C revealed the lowest resistance among the four junctions at each annealing temperature. The interface resistance was estimated to be 0.079, 0.073, 0.080, 0.098, and $0.199\,\Omega\,\mathrm{cm}^2$ for this junction without and with annealing at 100, 200, 300, and 400 °C, respectively.

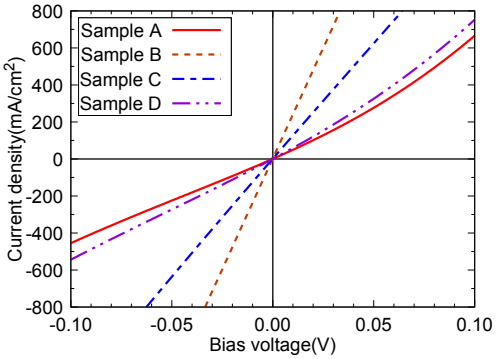

Fig. 5. (Color online) *I–V* characteristics of Samples A, B, C, and D measured at room temperature.

The relationships between the saturation current density J_s and the ambient temperature T for Samples E and F are shown in Figs. 7(a) and 7(b), respectively. The *I–V* characteristics measured at varied temperatures are shown in the inset of each figure. J_s at each temperature was determined by extrapolating the reverse-bias *I–V* characteristics to 0 V. As is shown in Fig. 7(a), $\ln(J_s/T^2)$ of Samples E revealed an excellent linear fit on $1000/T$ between 250 and 474 K. Figure 7(b) showed that $\ln(J_s/T^2)$ linearly depended on T between 350 and 475 K in Sample F. Such linear dependences suggested that the electrical conduction was dominated by the thermionic emission of carriers. From the slope of the linear fitting, the barrier heights of Samples E and F were estimated to be 0.63 and 0.51 eV, respectively. At lower temperatures, a combination of tunneling and generation–recombination process was likely to be a major mechanism of the conduction since the dependence of $\ln(J_s/T^2)$ on the temperature was weak.

4. Discussion

The carrier concentration of ITO films suggests that ITO is regarded as an n^{++}-type degenerate semiconductor. In addition, the changes in their resistivities were small against annealing at temperatures up to 400 °C. Consequently, the influence of the resistivity of ITO on Si substrates is likely to be small for the interface resistance of GaAs//ITO/Si junctions, although the electrical conduction in all of the GaAs//ITO/Si junctions was significantly degraded with the increase in annealing temperature. The observed increase in the interface resistance in the GaAs//ITO/Si junctions suggests that the potential barrier heights of the GaAs//ITO bonding interfaces and/or the Si/ITO interfaces could be increased by the annealing.

Regardless of the mechanism of the change in the interface resistance, it is notable that the interface resistances of n^+-GaAs//ITO/n^+-Si and p^+-GaAs//ITO/n^+-Si junctions with annealing at 400 °C are still lower than those of InGaP/

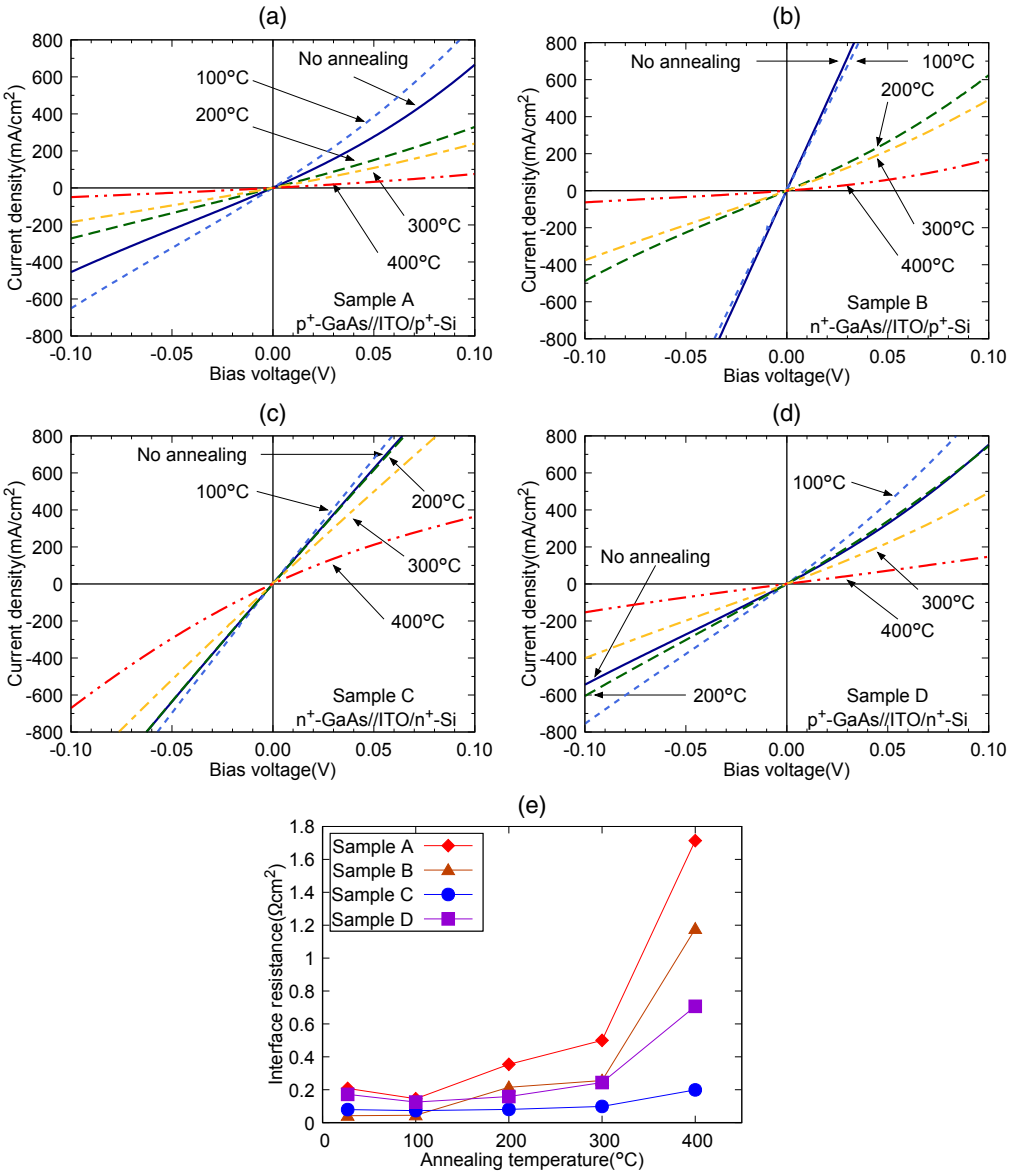

Fig. 6. (Color online) *I–V* characteristics of Samples (a) A, (b) B, (c) C, and (d) D with annealing at different temperatures measured at room temperature and (e) resistance of the respective samples as a function of annealing temperature.

GaAs/Si hybrid triple-junction cells, which we previously reported.[15] Furthermore, the interface resistances of GaAs//ITO/Si junctions are sufficiently low for application in concentrator photovoltaics.[31] These results indicate that SAB-based n^+-GaAs//ITO bonding interfaces with ITO intermediate layers have great potential to reduce the series resistance in III–V/Si hybrid triple-junction solar cells.

Here, we regard the ITO//GaAs junction as a metal/semiconductor junction since the carrier concentration of ITO films is much higher than those of n-GaAs and p-GaAs epitaxial layers. In addition, we assume that there are no extra charges due to the interface states at the bonding interfaces and that the Fermi level of ITO coincides with its conduction band edge. On the basis of these assumptions, we estimate the energy-band diagrams of the ITO//n-GaAs and ITO//p-GaAs bonding interface at zero bias voltage and room temperature, which are shown in Figs. 8(a) and 8(b), respectively. The barrier height of Sample F (n-GaAs//ITO/n^+-Si junction, 0.51 eV) is found to be lower than the barrier height reported for evaporated ITO/n-GaAs Schottky diodes, which was between 0.70 and 0.78 eV,[32] and that reported for sputtered ITO/n-GaAs Schottky diodes (0.82 eV[33]). The difference might be attributed to the damage introduced at the interfaces during the FAB irradiation.

The width of the depletion layer (W_D) in GaAs layers is given by

$$W_D = \sqrt{\frac{2\varepsilon_0\varepsilon_s\phi_{bi}}{qN_{D(A)}}}, \quad (2)$$

where ε_0 and ε_s are the permittivity of vacuum and the static dielectric constant of GaAs, respectively, $N_{D(A)}$ is the concentration of donors (acceptors) in n-GaAs (p-GaAs) epitaxial layers, and ϕ_{bi} is the built-in potential of the ITO/n-GaAs and ITO/p-GaAs bonding interface, which is simply the difference between the work function of ITO and n-GaAs and p-GaAs. The width of the depletion layer on the GaAs side of ITO/n-GaAs and ITO/p-GaAs junctions was calculated to be 36.3 and 40.3 nm, respectively.

By assuming that the band offsets of ITO//heavily doped GaAs junctions are the same as those given in Figs. 8(a) and

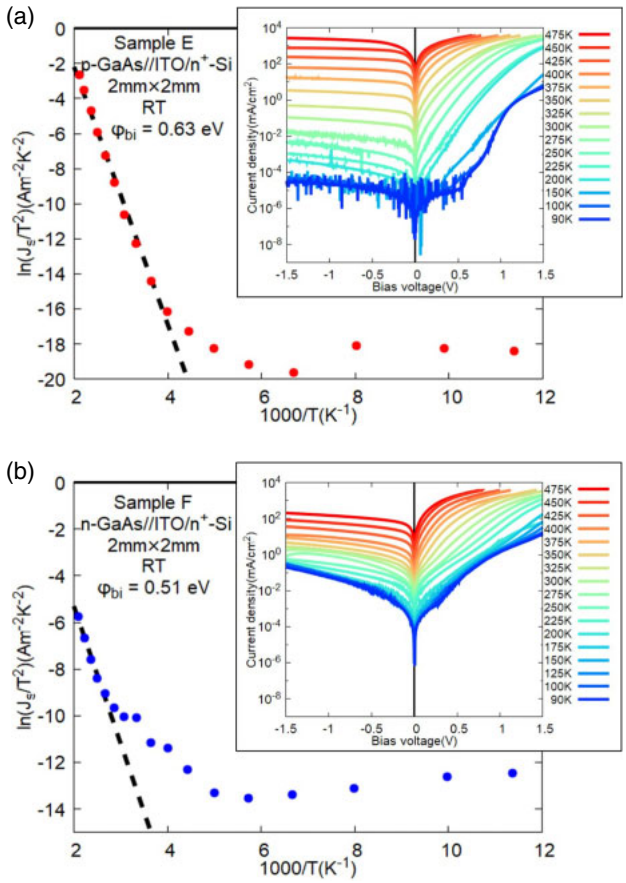

Fig. 7. (Color online) Arrhenius plot of $\ln(J_s/T^2)$ versus $10^3/T$ showing the temperature dependence of thermionic emission current in samples (a) E and (b) F. The inset shows the *I–V* characteristics of the respective samples measured at temperatures between 90 and 475 K.

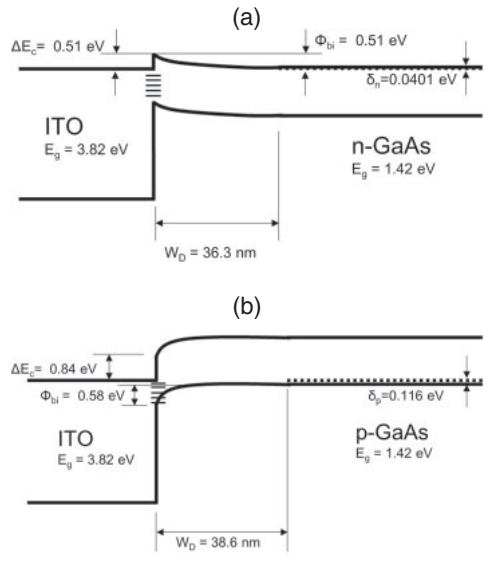

Fig. 8. Schematic energy-band diagrams of (a) ITO/n-GaAs and (b) ITO/p-GaAs interfaces.

8(b), the width of the depletion layer on the GaAs side of ITO//n^+-GaAs and ITO//p^+-GaAs junctions was calculated to be 3.63 and 4.03 nm, respectively. This is because the carrier concentration is two orders of magnitude larger in the heavily doped GaAs layers. The narrower depletion layer in the ITO//n^+-GaAs is assumed to enable the carriers to more effectively tunnel across the depletion layer of ITO//n^+-GaAs junctions in comparison with that of ITO//p^+-GaAs junctions. Such a scheme is in agreement with the measurement results of *I–V* characteristics, that is, the interface resistance of the n^+-GaAs//ITO/Si junction is lower than that of the p^+-GaAs//ITO/Si junction. Similar results were observed in ITO/n^+-Si and ITO/p^+-Si junctions.[27)]

In the this work, we have used 100-nm-thick ITO films to examine both the structural and electrical properties of GaAs//ITO/Si junctions. As shown in Fig. 2(c), the α of ITO films for wavelengths around 900 nm is approximately $10^4\,cm^{-1}$. Consequently, the optical absorption for such wavelengths due to the 100-nm-thick ITO films is estimated to be as high as ~10%. In addition, the reflection at GaAs/ITO and ITO/Si interfaces in GaAs//ITO/Si junctions is likely to decrease the magnitude of incident light on underlying Si layers. These contentions explain our previous result that the internal quantum efficiencies of the Si bottom cells in InGaP/GaAs//ITO/Si 3J cells were lower than those of the bottom cells in triple-junction cells without ITO intermediate layers.[28)] Given that the carrier density in ITO films is as high as $\sim 10^{21}\,cm^{-3}$, thinner (20 nm for example) ITO films are likely to efficiently work as conductive intermediate layers in 3J cells.

5. Conclusions

We fabricated p^+-GaAs//ITO/n^+-Si, n^+-GaAs//ITO/n^+-Si, p^+-GaAs//ITO/p^+-Si, n^+-GaAs//ITO/n^+-Si, n-GaAs//ITO/n^+-Si, and p-GaAs//ITO/n^+-Si junctions by bonding ITO films deposited on Si substrates to GaAs epitaxial layers using SAB. We measured the *I–V* characteristics of the n-GaAs//ITO/n^+-Si and p-GaAs//ITO/n^+-Si junctions at various ambient temperatures. The barrier heights of the n-GaAs//ITO/n^+-Si and p-GaAs//ITO/n^+-Si junctions were estimated to be 0.51 and 0.63 eV, respectively, by analyzing the dependences of the saturation current on ambient temperature. The barrier height of n-GaAs//ITO/n^+-Si junctions, 0.51 eV, was slightly lower than those reported for ITO/n-GaAs Schottky diodes made of evaporated and sputtered ITO films. The difference might be due to the damage introduced at the bonding interfaces.

We also measured the room-temperature *I–V* characteristics of the p^+-GaAs//ITO/p^+-Si, n^+-GaAs//ITO/p^+-Si, n^+-GaAs//ITO/n^+-Si, and p^+-GaAs//ITO/n^+-Si junctions after annealing. For each junction, we observed larger interface resistances for higher annealing temperatures. The n^+-GaAs//ITO/n^+-Si junction showed the lowest interface resistance among the junctions annealed at 400 °C. The obtained interface resistance for this junction was lower than that estimated for the GaAs/Si interfaces in the actual hybrid triple-junction cells. These results demonstrated that the n^+-GaAs//ITO/n^+-Si junction with an ITO intermediate layer could be effective for reducing series resistance in hybrid multijunction cells.

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