GaAs/Si Double-Junction Cells Fabricated by Sacrificial Layer Etching of Directly-Bonded III-V/Si Junctions

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***Abstract*—A GaAs/Si double-junction cell is fabricated by directly bonding a GaAs single-junction cell structure grown on a GaAs (001) substrate to a n-on-p Si subcell and separating the GaAs substrate using a sacrificial layer etching. Before the sacrificial layer etching, the III-V/Si junction is annealed at 300 °C for 1 hour so as to recrystallize the interface and achieve an enough bonding strength based on the results of hard X-ray photoemission spectroscopy. We obtain a bonding yield of ~80% after the sacrificial layer etching. We confirm that the fabricated double-junction cell normally operates by measuring its current-voltage and spectral-response characteristics.**

I. Introduction

III-V/Si hybrid multijunction cells are promising so as to realize high-efficiency and low-cost photovoltaics. We previously reported on InGaP/GaAs/Si [1] and InGaP/GaAs/ITO/Si [2] multijunction cells. Recently efficiencies higher that >30% was achieved by optimizing the layer structures [3]. In the simplest process sequence for fabricating such multijunction cells, III-V epi layers grown on GaAs substrates are directly bonded to bottom cell structures that are fabricated on Si substrates in advance. The surface-activated bonding (SAB) technologies are widely used. After removing the GaAs substrates, multijunction cells are fabricated on the remaining III-V epi layer/Si junctions.

The removed GaAs substrate should be reused for the epitaxial growth so as to minimize the cost of photovoltaics. Thin AlAs layers inserted between GaAs substrates and III-V epi layers are typically used as sacrificial layer for separating the GaAs substrate from the epi layers since the AlAs layers are selectively etched in a HF etchant.

We recently reported on measurements of hard X-ray photoemission spectroscopy (HAXPES) of SAB-based thin GaAs/Si junctions [4]. We found that the signals due to oxygen were dominant at the as-bonded GaAs/Si interfaces, while the contribution of the oxygen decreased by a short-period (1 min.) annealing at 300 °C. This result suggested that the annealing brought about the recrystallization at the interface.

In this work, we examined the contribution of such an annealing for a longer period by means of HAXPEX. Based on the results, we annealed III-V epi substrate/Si substrate junctions that we had fabricated by using the SAB. AlAs sacrificial layers had been sandwiched between the epi layers and GaAs substrates. GaAs/Si double-junction cells were fabricated after separating the GaAs substrate using the sacrificial layer etching. The performances of such double-junction cells were compared with those fabricated through the conventional device process.

II. Method

On a GaAs (100) substrate, we grew a ≈250-nm-thick undoped InGaP layer and a ≈20-nm-thick undoped GaAs layer in this sequence. The prepared epi-substrate was attached to n-Si substrate by the SAB without heating. The fabricated junctions were separated into two pieces. They were annealed at 300 ˚C for 1 min and for 1 hour, respectively. The GaAs substrate and the undoped InGaP layer were removed from each piece by polishing and wet etching so as to prepare undoped GaAs/n-Si junctions. The Ga2p core spectra of the two junctions were measured using BL47XU of SPring-8, JASRI with an energy of incident photons of 8 keV and a take-off angle between 4 and 76 °.

We also prepared a GaAs epi-substrate composed of an AlAs sacrificial layer and a GaAs single-junction cell structure grown on a GaAs (100) substrate. The epi-substrate was bonded to an n-on-p Si subcell structure as well as an n^+-Si substrate. The bonding area was 10 mm × 12 mm. After annealing the junctions, the AlAs sacrificial layer was selectively etched and the GaAs substrate was separated by applying a force to a side of the GaAs substrate in a HF etchant. The condition of the annealing was fixed with reference to the results of HAXPES analysis as is discussed below. We fabricated 4 mm^2 (2 mm × 2 mm) GaAs single-junction cells on Si substrates and GaAs/Si double-junction cells by the mesa etching of III-V layers and formation of emitter and base contacts. For comparison we also fabricated the double-junction cells using a conventional process, i.e., by removing the GaAs substrate from the junctions by grinding and etching. Note that neither anti-reflection films or textures were formed. The structures of fabricated GaAs single-junction and GaAs/Si double-junction cells are schematically shown in Figs. 1(a) and 1(b), respectively.

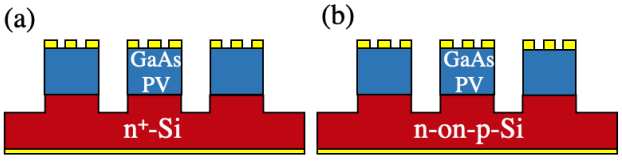

Fig. 1. A schematic cross section of (a) a GaAs single junction cell bonded to an n^+-Si substrate and (b) a GaAs/Si double-junction cell.

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We measured the current-voltage (I-V) and spectral-response characteristics of the fabricated cells. The I-V characteristics were measured under a solar irradiance of an air mass of 1.5G and one sun. In addition, the surface of the separated GaAs substrate was observed by an atomic force microscopy (AFM).

III. RESULTS AND DISCUSSIONS

A. Results of HAXPES

Figures 2(a) and 2(b) show the Ga2p core spectra at TOA of 76° of the ≈20-nm GaAs/Si junctions annealed for 1 min. and 1 hour, respectively. We found by the least-squares method that each spectrum was composed of two peaks. The peaks at 1118.5 and 1116.9 eV were attributed to the Ga-O and Ga-As bonds, respectively. We found that the area of Ga-O signal to the area of Ga-As signal was lower in the spectrum of junction annealed for 1 hour. This result suggested that the recrystallization of amorphous layers due to the surface activation proceeded and the tolerance of the bonding interfaces against the device process was improved by annealing the junctions for a longer period, i.e., it was assumed that the III-V/Si junctions should be annealed for a longer period before selectively etching the sacrificial layers. In this work, based on the results of HAXPES measurements, the III-V/Si junctions employed for fabricating cells were annealed at 300 ℃ for 1 hour before separating the GaAs substrates.

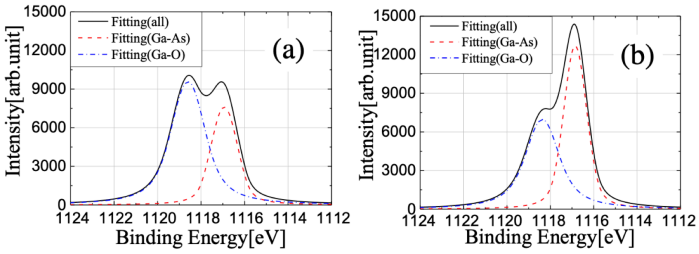

Fig. 2. Ga2p core spectra of ≈20-nm GaAs/Si junctions (a) annealed at 300 ℃ for 1 min. and (b) annealed at 300 ℃ for 1 hour.

B. Fabrication and Characterization of GaAs Single-Junction Cells on Si and GaAs/Si Double-Junction Cells

We found that the period for the sacrificial layer etching was ≈24 hours so as to separate the GaAs substrate from a 1 cm×1.2 cm III-V/Si junction. A photo of the GaAs single-junction cell structure bonded to a Si substrate after completing the sacrificial layer etching is shown in Fig. 3(a). A ~100-mm^2 GaAs cell layer, i.e., a ~80% of initially bonded area remained bonded to the Si substrate after separating GaAs the substrate. We confirmed that the yield of the GaAs single-junction cell structure was largely improved by annealing the junctions for 1 hour.

An AFM image of the surface of the separated GaAs substrate is shown in Fig. 3(b). The averaged roughness of the surface was 0.25 nm, which was similar to that of epi-ready GaAs substrates. This result suggests that GaAs substrates might be potentially able to be recycled by combining the SAB and the sacrificial layer etching.

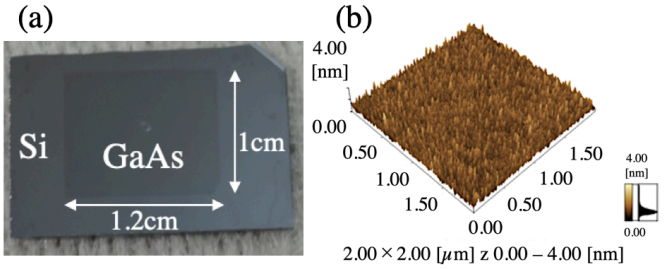

Fig. 3. (a) A photo of GaAs single-junction cell structure bonded to a Si substrate after completing the sacrificial layer etching. (b) An AFM image of a GaAs substrate separated from the III-V/Si junction by means of the sacrificial layer etching.

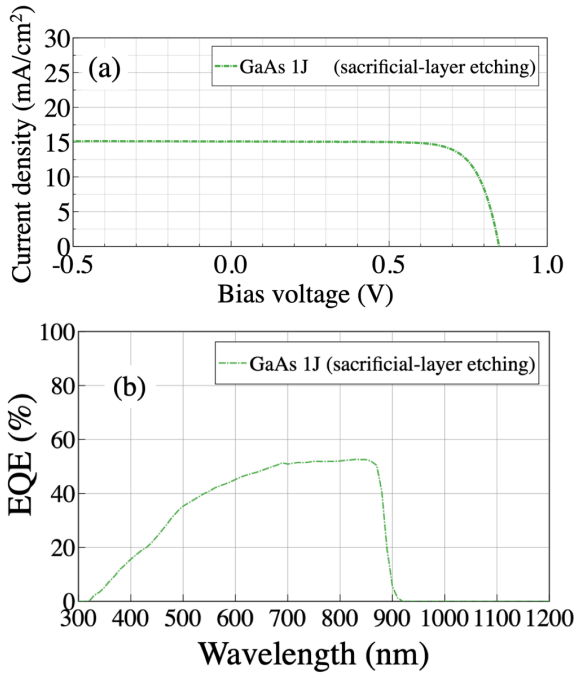

Fig. 4. (a) The I-V characteristics and (b) EQE spectrum of a GaAs single-junction cells on an n+-Si substrate.

The I-V characteristics and the external quantum efficiency (EQE) spectrum of a GaAs single-junction cell on an n+-Si substrate are shown in Figs. 4(a) and 4(b), respectively. The short-circuit current (J_{SC}), open-circuit voltage (V_{OC}), fill factor (FF), and conversion efficiency (η) were 15.1 mA/cm^2, 0.85 V, 76%, and 9.8%, respectively.

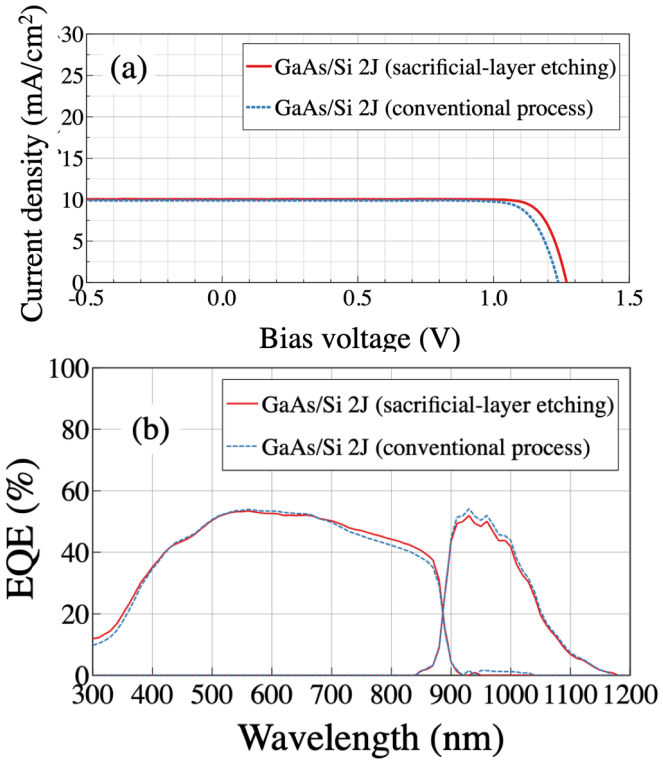

Fig. 5. (a) The I-V characteristics and (b) EQE spectra of GaAs/Si double-junction cells.

TABLE I
SUMMARY OF CHARACTERISTICS OF GAAS/SI DOUBLE-JUNCTION CELLS

	Jsc (mA/cm^2)	Voc (V)	FF	η (%)
2J (sacrificial-layer etching)	10.0	1.27	0.84	10.7
2J (conventional process)	9.9	1.24	0.82	10.1

Figures 5(a) shows the I-V characteristics of a GaAs/Si double-junction cell fabricated using the sacrificial layer etching and the characteristics of a double-junction cell fabricated using the conventional process. Figures 5(b) compares the EQE spectra of the two types of the double-junction cells. Their J_{SC}, V_{OC}, FF, and η are summarized in Table I. The lower J_{SC} of the double-junction cells (10.0 mA/cm^2) in comparison with the GaAs single-junction cell was attributed to the mismatching in currents between the GaAs and Si subcells. The higher V_{OC} (1.27 V) and the EQE spectra indicate that the fabricated GaAs/Si double junction cells revealed a normal operation. It is notable that the characteristics of the two types of the double-junction cells were similar to each other. The results indicate that the sacrificial layer etching of the III-V/Si junctions is a practically useful method for fabricating hybrid multijunction solar cells.

IV. CONCLUSION

We fabricated GaAs/Si double-junction cells by means of the surface-activated bonding (SAB) of GaAs and Si single-junction cell structures and the sacrificial layer etching. The III-V/Si junctions were annealed for 1 hour so that an enough bonding yield (~80%) was realized after the sacrificial layer etching. The roughness average of the surface of GaAs substrate separated from the junction was ≈0.25 nm. The cell characteristics demonstrated that the fabricated cells normally operated. These results indicated that the combination of the sacrificial layer etching and SAB is potentially applicable for fabricating III-V/Si multijunction cells while compound semiconductor substrates are recycled.

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