ECS Transactions, 64 (5) 235-242 (2014)
10.1149/06405.0235ecst ©The Electrochemical Society

Type-II Band Profile of GaAs/Si Hetero Junctions by Surface Activated Bonding for Hybrid Tandem Cells

Naoteru Shigekawa[a], Jianbo Liang[a], Masashi Morimoto[a], and Shota Nishida[a]

[a] Department of Applied Physics and Electronics, Graduate School of Engineering, Osaka City University, Osaka 558-8585, Japan

We fabricated p^+-GaAs/n-Si and n^+-GaAs/p-Si junctions by using surface activated bonding and measured their current-voltage and capacitance-voltage characteristics at room temperature. Their conduction band offset, which was extracted from the capacitance-voltage characteristics, was 0.57-0.84 eV. The results suggested that the band profiles of junctions had type-II features, which was likely to be preferable for fabricating low-resistance tunnelling junctions in hybrid tandem cells. The influence of possible interface states on the electrical properties of junctions was also discussed using the charge neutral level model.

Introduction

Tandem cells made of compound-semiconductor-based sub cells with different band gaps are promising as high-efficiency next-generation solar cells (1). From the practical viewpoints Si-based cells should be used as bottom cells instead of cells grown on GaAs or InP substrates. Given that the growth of III-V materials on Si substrates is still difficult technical issues because of the difference in thermal expansion coefficients and lattice constants (2) as well as the frequent occurrence of anti-phase domain (3), the hybrid approach employing the direct wafer bonding is attractive. The present authors reported on the characteristics of InGaP-on-Si and InGaP/GaAs-on-Si tandem cells (4,5) that had been fabricated by surface-activated bonding (SAB). The efficiency of the InGaP/GaAs/Si tandem cells was 24.4% (5). The key issue in fabricating such tandem cells lies in formation of low-parasitic-resistance tunnelling junctions made of III-V-materials, typically GaAs, and Si. The band profile of junctions, which dominantly determines the transport characteristics of carriers across the interfaces, must be clarified.

Interface states are introduced at the bonding interfaces in junctions made by the direct wafer bonding. Their electrical characteristics were analysed by using the charge neutral level (CNL) model, in which interface states with energies lower (higher) than the energy of the CNL E_{CNL} are assumed to have donor-like (acceptor-like) features (6). The Fermi level at the interface relative to E_{CNL} determines the density of electrical charges at the interface Q_{it}. The influence of the interface charges was investigated for bonding based Si/Si junctions (7). The present authors reported that traps at the interface played a major role in the carrier transport properties in SAB-based p-Si/n-Si junctions (8).

In this work, we fabricated p^+-GaAs/n-Si and n^+-GaAs/p-Si hetero junctions by SAB. We measured their current-voltage (I-V) and capacitance-voltage (C-V) characteristics

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and extracted the band offset of respective junctions. The possible influence of interface charges to the measured band offset was also discussed.

Experiments

We employed (100) p$^+$-GaAs (a concentration of acceptors of ~1×10^{19} cm^{-3}), (100) n-Si (a concentration of donors of 4.8×10^{16} cm^{-3}), (100) n$^+$-GaAs (1.1×10^{18} cm^{-3}), and (100) p-Si (2.4×10^{17} cm^{-3}) substrates for fabricating p-GaAs/n-Si and p-Si/n-GaAs junctions. The impurity concentrations and the Fermi levels in the respective substrates, which are hereafter referred to as (N_{A1}, δ_{p1}), (N_{D2}, δ_{n2}), (N_{D1}, δ_{n1}), and (N_{A2}, δ_{p2}) for p$^+$-GaAs, n-Si, n$^+$-GaAs, and p-Si substrates, respectively, are summarised in Table I. The Fermi levels are defined as separation from the conduction-band (valence-band) edges in n- (p-) type substrates. p$^+$-GaAs/n-Si and n$^+$-GaAs/p-Si junctions were formed by bonding the substrates to each other after their surfaces were activated by Ar beam irradiation in a high vacuum. The background pressure prior to the Ar beam irradiation and the bonding pressure were ~10^{-6} Pa and ~10 MPa, respectively. After bonding, ohmic contacts were formed by evaporating AuZn/Ti/Au, Ti/Au, AuGe/Ni/Ti/Au, and Al/Ni/Au films on the backsides of the p-GaAs, n-Si, n-GaAs, and p-Si substrates, respectively, and annealing (400 °C, 1min. in N2 ambient). Then the junctions were diced into 2-mm by 2-mm pieces. Their I-V and C-V characteristics were measured at room temperature. The frequency for C-V measurements was 100 kHz.

TABLE I. Impurity concentrations and Fermi levels of substrates employed in the work.

Substrate	Impurity concentration (cm^{-3})	Fermi level (meV)
p$^+$-GaAs	$(N_{A1} =)$ ~1×10^{19}	$(\delta_{p1} =)$ 3
n-Si	$(N_{D2} =)$ 4.8×10^{16}	$(\delta_{n2} =)$ -168
n$^+$-GaAs	$(N_{D1} =)$ 1.1×10^{18}	$(\delta_{n1} =)$ 22
p-Si	$(N_{A2} =)$ 2.4×10^{17}	$(\delta_{p2} =)$ -111

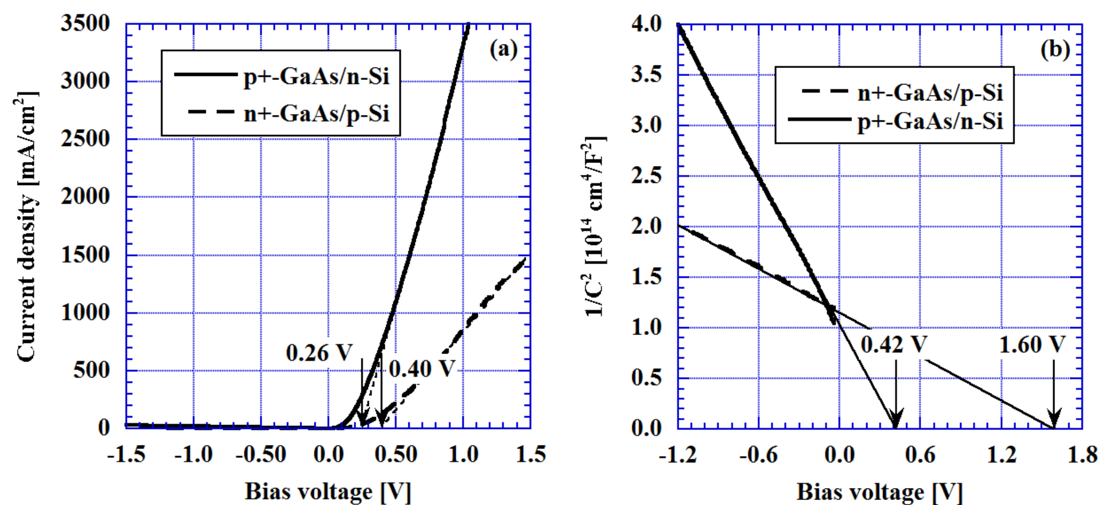

Figure 1. (a) Current-voltage and (b) capacitance-voltage characteristics of the p$^+$-GaAs/n-Si and n$^+$-GaAs/p-Si junctions that we fabricated. Onsets of currents for forward-bias and flat-band voltages are also shown.

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I-V characteristics of the junctions are shown in Fig. 1(a). Both characteristics showed rectifying properties. The onset of currents for forward bias voltages was found to be 0.26 and 0.4 V for the p^+-GaAs/n-Si and n^+-GaAs/p-Si junctions, respectively. Their $1/C^2$-V characteristics are shown in Fig. 1(b). We find that each curve reveals an almost straight line. The flat-band voltage V_{FB} was extracted to be 0.42 and 1.60 V in the p^+-GaAs/n-Si and n^+-GaAs/p-Si junctions, respectively, by linearly extrapolating the $1/C^2$-V characteristics. The lower flat-band voltage observed in the p^+-GaAs/n-Si junction was in accordance with the smaller onset in its I-V characteristics. Similarly to results for SAB-based p-Si/n-Si (8) and wafer-fused p-GaAs/n-GaN (9) junctions, the onset in the I-V characteristics of each junction is systematically smaller than the predicted flat-band voltage, which suggests that the contribution of interface states to the electrical conduction cannot be negligible.

Slopes of the $1/C^2$-V characteristics are -2.5×10^{14} and -0.7×10^{14} $cm^4/[F^2\cdot V]$ for p^+-GaAs/n-Si and n^+-GaAs/p-Si junctions, respectively. By ignoring the contribution of the interface charges, the slope is modelled as

$$\frac{d}{dV}\left(\frac{1}{C^2}\right) = -\frac{2}{q}\left(\frac{1}{\varepsilon_1 N_{(\mathrm{A\ or\ D})1}} + \frac{1}{\varepsilon_2 N_{(\mathrm{D\ or\ A})2}}\right), \qquad [1]$$

where q is the elementary electric charge. ε_1 and ε_2 are the dielectric constants of GaAs and Si. Using this equation, the magnitudes of the slope were estimated to be -2.45×10^{14} and -0.60×10^{14} $cm^4/[F^2\cdot V]$ for the p^+-GaAs/n-Si and n^+-GaAs/p-Si junctions, respectively. These results are in an agreement with measurements.

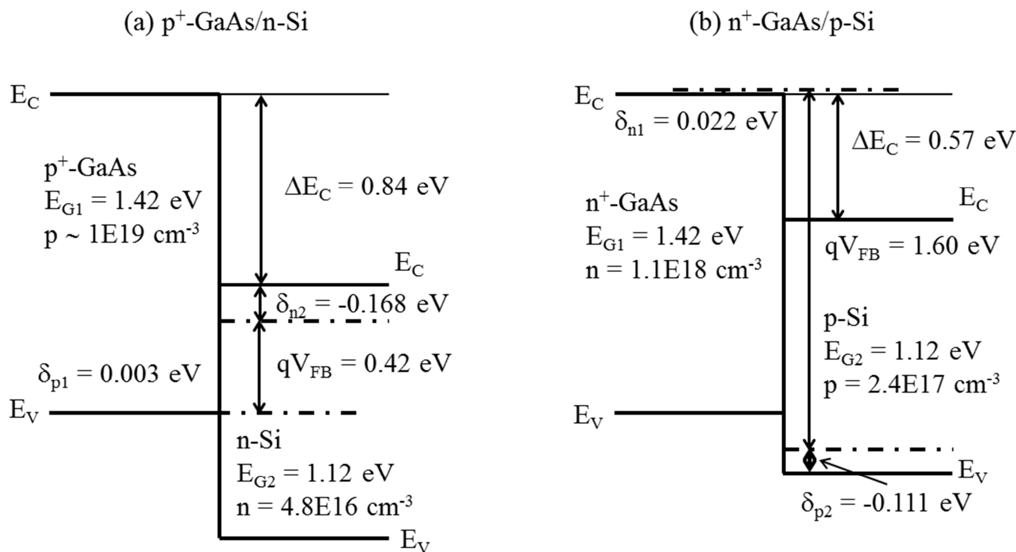

Figure 2. The band profiles in the flat band condition of the (a) p^+-GaAs/n-Si and (b) n^+-GaAs/p-Si junctions.

The conduction band offset ΔE_C between GaAs and Si is expressed as,

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$$\Delta E_C = \delta_{p1} + \delta_{n2} + E_{G1} - qV_{FB}, \quad [2]$$

and

$$\Delta E_C = qV_{FB} - (\delta_{n1} + \delta_{p2} + E_{G2}), \quad [3]$$

for p^+-GaAs/n-Si and n^+-GaAs/p-Si junctions, respectively. E_{G1} and E_{G2} stand for band gaps of GaAs and Si. Using these expressions, ΔE_C was estimated to be 0.84 and 0.57 eV for the p^+-GaAs/n-Si and n^+-GaAs/p-Si junctions, respectively. ΔE_C obtained for the n^+-GaAs/p-Si junctions is close to a previous report for the bonding interfaces in n-GaAs/n-Si junctions (10). The obtained ΔE_C values disagree with an estimation based on a simple view that the conduction band offset is given by the difference in electron affinities between Si and GaAs, both of which are ≈ 4 eV. The discrepancy between the measurements and the estimation based on the electron-affinity difference is likely to be attributed to the heterovalent properties in GaAs/Si junctions (11, 12). The band profiles obtained for the respective junctions in the flat band condition are shown in Figs. 2(a) and 2(b). We find that the band profile reveals type-II features in the both junctions.

Theoretical analysis using CNL model

In order to reconcile two different ΔE_C values deduced for the p^+-GaAs/n-Si and n^+-GaAs/p-Si junctions, we analyse the influence of the interface charges on the C-V characteristics of the respective junctions. The analysis is based on the following assumptions.

(i) The states are uniformly distributed in the overlap of band gaps of GaAs and Si layers. The density of the interface states D_{it} is, consequently, independent of their energy.

(ii) The distribution of charges in the more heavily doped layer (GaAs for the present work) is locally determined by solving Poisson equation. The distribution of charges in the more lightly doped layer (Si) is estimated by using the depletion layer approximation.

(iii) The charge neutral condition holds, i.e., the sum of the sheet charge densities in the respective layers and that at the interface is zero irrespective of the bias voltage.

(iv) Given that $1/C^2$-V characteristics that we measured revealed almost straight lines and their slope was in agreement with that expected from eq. [1], Q_{it} is assumed to be independent of V and remain equal to that for $V = 0$ V when the junctions are biased. This means that the interface charges were treated as fixed charges. Further evaluations of band profiles in biased junctions should be performed for achieving a clear evidence for this assumption.

In the case of p^+-GaAs/n-Si junctions (see Fig. 3), the bias voltage, which is negative when the junctions are reverse-biased, is expressed as

$$V = \frac{1}{q}\left(\delta_{p1} + E_{G1} - \Delta E_C + \delta_{n2}\right) - \psi_S - \frac{qN_{D2}}{2\varepsilon_2} w_2{}^2. \quad [4]$$

In this equation, ψ_S is the surface potential of the p+-GaAs layer. ε_2 and w_2 are the dielectric constant and thickness of depletion layer in the n-Si layer, respectively.

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Using the assumption (i), Q_{it} is given by

$$Q_{it} = qD_{it}\left[\int_{\delta_{p1}-q\psi_S}^{\delta_{p1}-q\psi_S+E_{CNL}} dE\left\{1-\frac{1}{1+\exp(\beta E)}\right\} - \int_{\delta_{p1}-q\psi_S+E_{CNL}}^{\delta_{p1}-q\psi_S+E_{g1}-\Delta E_C} dE\frac{1}{1+\exp(\beta E)}\right]$$

$$= \frac{qD_{it}}{\beta}\left[\ln\frac{1+\exp[\beta(\delta_{p1}-q\psi_S+E_{CNL})]}{1+\exp[\beta(\delta_{p1}-q\psi_S)]} - \ln\frac{1+\exp[-\beta(\delta_{p1}-q\psi_S+E_{CNL})]}{1+\exp[-\beta(\delta_{p1}-q\psi_S+E_{g1}-\Delta E_C)]}\right]. \quad [5]$$

Here β is the inverse of temperature.

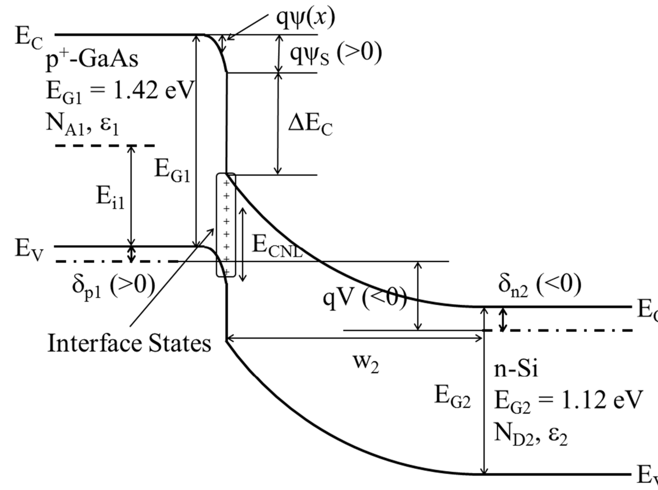

Figure 3. Schematic band diagram of a p+-GaAs/n-Si junction.

Using the intrinsic Fermi level in the p+-GaAs layer measured from the valence band edge E_{i1} and the intrinsic carrier concentration n_{i1}, concentrations of the majority holes and minority electrons in the deep inside of the p+-GaAs layer are $n_{i1}\exp[\beta(E_{i1}+\delta_{p1})]$and $n_{i1}\exp[-\beta(E_{i1}+\delta_{p1})]$, respectively. Their difference should be equal to the concentration of acceptors N_{A1}. Concentrations of carriers at a position close to the interface x are $n_{i1}\exp[\beta(E_{i1}+\delta_{p1}-q\psi(x))]$ (holes) and $n_{i1}\exp[-\beta(E_{i1}+\delta_{p1}-q\psi(x))]$ (electrons), respectively, using the channel potential $\psi(x)$. Poisson equation in the p+-GaAs layer is, then, given by

$$\frac{d^2}{dx^2}\psi(x) = -\frac{2qn_{i1}}{\varepsilon_1}\left[\sinh\left(\beta\left(E_{i1}+\delta_{p1}-q\psi(x)\right)\right) - \sinh\left(\beta\left(E_{i1}+\delta_{p1}\right)\right)\right]. \quad [6]$$

By integrating this equation from $x=-\infty$ to $x=0$ (the interface) and applying Gauss law, we obtain the relationship between the sheet charge density in the GaAs layer Q_{GaAs} and the surface potential ψ_S. Q_{GaAs} is negative (positive) when ψ_S is positive (negative), or when the band of GaAs is bent downward (upward).

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$$Q_{GaAs} = \pm\left[(4\varepsilon_1 q n_{i1})\left\{\sinh\left(\beta\left(E_{i1}+\delta_{p1}\right)\right)\psi_S + \frac{1}{\beta q}\left\{\cosh\left(\beta\left(E_{i1}+\delta_{p1}-q\psi_S\right)\right)-\cosh\left(\beta\left(E_{i1}+\delta_{p1}\right)\right)\right\}\right\}\right]^{1/2}. \quad [7]$$

The charge density in the Si layer Q_{Si} is simply given by $Q_{Si} = qN_{D2}w_2$. By combining these equations with the charge neutral condition ($Q_{GaAs} + Q_{Si} + Q_{it} = 0$), we first obtain Q_{it} for the zero-bias voltage (V = 0 V). Next the relationship between the bias voltage and the capacitance in the junction is achieved by using the zero-bias value for Q_{it}.

For n$^+$-GaAs/p-Si junctions, Q_{it} and Q_{GaAs} are expressed as

$$Q_{it} = \frac{qD_{it}}{\beta}\left[\ln\frac{1+\exp[-\beta(\delta_{n1}+E_{g1}+q\psi_S-E_{CNL})]}{1+\exp[-\beta(\delta_{n1}+E_{g1}+q\psi_S)]} - \ln\frac{1+\exp[\beta(\delta_{n1}+E_{g1}+q\psi_S-E_{CNL})]}{1+\exp[\beta(\delta_{n1}+q\psi_S+\Delta E_C)]}\right], \quad [8]$$

and

$$Q_{GaAs} = \pm\left[(4\varepsilon_1 q n_{i1})\left\{\frac{1}{\beta q}\left\{\cosh\left(\beta\left(\delta_{n1}+E_{g1}-E_{i1}+q\psi_S\right)\right)-\cosh\left(\beta\left(\delta_{n1}+E_{g1}-E_{i1}\right)\right)\right\}\right\} - \sinh\left(\beta(E_{i1}+\delta_{n1})\right)\psi_S\right]^{1/2}, \quad [9]$$

respectively. Q_{Si} is simply given by $Q_{Si} = -qN_{A2}w_2$. The C-V characteristics are calculated using these equations through a process similar to that for p$^+$-GaAs/n-Si junctions.

Three cases of ΔE_C = 0.57, 0.70, and 0.84 eV, extracted values of ΔE_C and their average, were considered. E_{CNL} was fixed to be 0.5 eV (6). Figure 4(a) shows the relationships between Q_{it}/q on D_{it} at $V = 0$ V for p$^+$-GaAs/n-Si and n$^+$-GaAs/p-Si junctions. The dependencies of V_{FB} on D_{it} for the respective junctions are shown in Fig. 4(b). In the unbiased p$^+$-GaAs/n-Si junction the Fermi level is below the CNL so that positive charges are built at the interface. The positive charges are compensated by negative space charges in the p$^+$-GaAs layer, which plays a role of lowering V_{FB}. In contrast, negative charges are distributed at the interface of the n$^+$-GaAs/p-Si junction, which brings about positive space charges in the n$^+$-GaAs layer and lowers V_{FB}.

We find from Fig. 4(b) that V_{FB} is shifted by several hundred mV when the interface states with densities of $10^{13\text{-}14}$ cm$^{-2}\cdot$eV^{-1} are introduced. Results shown in this figure suggest that the measured V_{FB} values for the two junctions might be explained by invoking charges in ~$10^{13\text{-}14}$ cm$^{-2}\cdot$eV^{-1} interface states in combination with a single ΔE_C value (say 0.7 eV). The contribution of the charges in the interface states to the shift of the optimum ΔE_C is schematically explained as follows: In the p$^+$-GaAs/n-Si junction with D_{it} of ~10^{13} cm$^{-2}\cdot$eV^{-1} and ΔE_C = 0.7 eV, the band profile in the p$^+$-GaAs layer is bent downwards, i.e., the negative charges are built, at the vicinity of the interface so as to cancel the contribution of the positive charges due to the interface states. When a bias voltage of 0.42 V is applied, the amount of these negative charges should be equal to that of the positive charges, so that the flat band condition is achieved. In contrast, in the n$^+$-

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GaAs/p-Si junction with D_{it} of ~10^{13} $cm^{-2}\cdot eV^{-1}$ and ΔE_C = 0.7 eV, the band profile in the n^+-GaAs layer is bent upwards, so that the flat band condition is achieved for a bias voltage of 1.6 V.

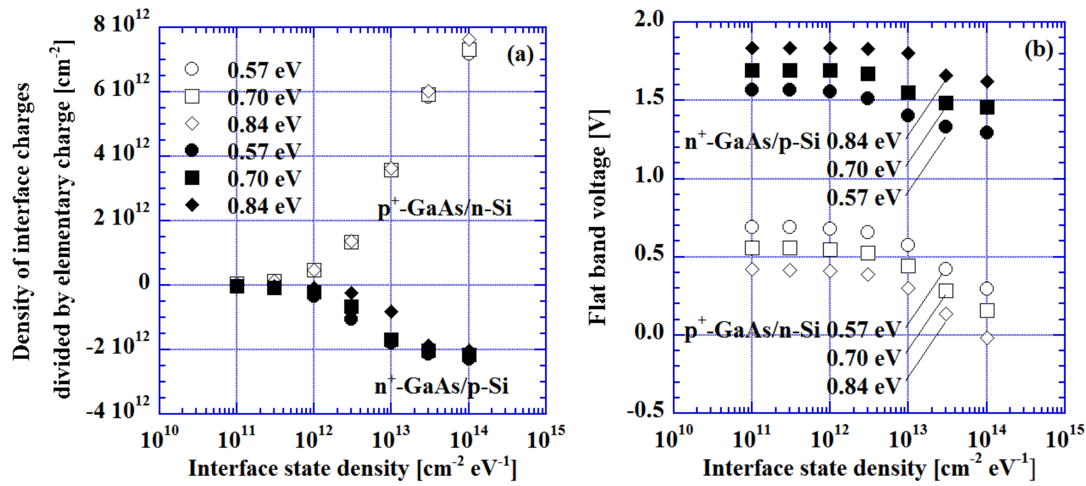

Figure 4. Dependencies of (a) Q_{it}/q at $V = 0$ V on D_{it} and of (b) V_{FB} on D_{it} in the p^+-GaAs/n-Si and n^+-GaAs/p-Si junctions.

Note that interface states with such densities could be formed in a device process using Ar beams such as dry etchings, which might show the validity of this scheme. Practically the result that the fabricated GaAs/Si junctions revealed type-II features with the higher conduction-band edges in GaAs layers suggests that p-GaAs/n-Si junctions are more preferable in comparison with n-GaAs/p-Si junctions for fabricating tunnel junctions in tandem cells since the overlap of band gaps is effectively smaller, which indicates that the resistance across the interface is lower, in p-GaAs/n-Si junctions.

Conclusion

We fabricated p^+-GaAs/n-Si and n^+-GaAs/p-Si junctions by using surface activated bonding. Their current-voltage (I-V) and capacitance-voltage (C-V) characteristics were measured at room temperature. We found that the flat band voltage in the C-V characteristics of the p^+-GaAs/n-Si junctions was lower than that of the n^+-GaAs/p-Si junctions, which was in consistent with the difference in the onset of the I-V characteristics. The conduction band offset ΔE_C was estimated to be 0.84 and 0.57 eV for the p^+-GaAs/n-Si and n^+-GaAs/p-Si junctions, respectively, from their flat band voltages on the assumption that the contribution of interface charges is negligible. One possible explanation for the difference between the two ΔE_C values was given in the framework of the charge neutral level model. The extracted ΔE_C suggested that GaAs/Si junctions revealed type-II features, which should play an important role in designing tunnel junctions with low parasitic resistances in III-V/Si hybrid tandem solar cells.

Acknowledgments

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The authors are grateful to T. Miyazaki for his assistance in sample fabrication and characterization. This work was supported by "Creative research for clean energy generation using solar energy" Programme of "Core Research for Evolutionary Science and Technology" (CREST) Scheme of Japan Science and Technology Agency (JST).

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