Japanese Journal of Applied Physics

The Japan Society of Applied Physics

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Japanese Journal of Applied Physics **57**, 02BE02 (2018)
https://doi.org/10.7567/JJAP.57.02BE02

REGULAR PAPER

Analysis of effects of interface-state charges on the electrical characteristics in GaAs/GaN heterojunctions

Shoji Yamajo, Jianbo Liang, and Naoteru Shigekawa*

Graduate School of Engineering, Osaka City University, Osaka 558-8585, Japan

*E-mail: shigekawa@elec.eng.osaka-cu.ac.jp

Received June 27, 2017; accepted September 21, 2017; published online December 28, 2017

Electrical properties of p^+-GaAs/n-GaN and n^+-GaAs/n-GaN junctions fabricated by surface-activated bonding are investigated by measuring their capacitance–voltage (C–V) and current–voltage (I–V) characteristics. The difference between their flat-band voltages (0.17 eV), which are extracted from C–V measurements, disagrees with the ideal value (1.52 V), suggesting that the Fermi level should be pinned at the bonding interface. The C–V characteristics of the two junctions are calculated by assuming that the Fermi level is pinned at the interface. The measured C–V characteristics quantitatively agree with modeled ones obtained by assuming that the interface state density and conduction band discontinuity are 1.5×10^{14} cm^{-2} eV^{-1} and 0.63 eV, respectively. The effective heights of barriers at interfaces, which we estimate by analyzing dependences of I–V characteristics on the ambient temperature, are ~10–20 meV for the two junctions at room temperature. This suggests that the transport of carriers is dominated by tunneling through interface states.

1. Introduction

Gallium nitride (GaN) is a promising component of next-generation power devices because of its high breakdown voltage, high thermal conductivity, and the high physical and chemical stabilities.[1,2] In contrast, GaAs has superior electron transport characteristics and is widely used in high-frequency devices because of its matured growth and process technologies.[3] Hence, the integration of GaAs and GaN enables us to fabricate unique electron devices for high-power and high-speed applications, which are otherwise unobtainable by either of the single materials. Here, we note that the energy band alignment of GaAs/GaN must be clarified so as to design devices using GaAs/GaN heterojunctions. Several authors reported on the growth of GaAs/GaN heterojunctions.[4–6] However, it is still difficult to epitaxially grow GaN layers on GaAs substrates. The quality of epitaxial layers was not satisfactory because of large differences in lattice constants and crystal structure between GaAs and GaN.[7–10] Furthermore, it was also reported that the nitrogen could diffuse across the GaAs/GaN interface during growth.[11] The resultant interfacial roughening of the GaAs/GaN interface together with the high dislocation density and other crystal defects was observed by scanning transmission electron microscope (STEM).[11]

One way to overcome these difficulties is direct wafer bonding processes such as wafer-fused bonding and surface-activated bonding (SAB).[3,12–15] In wafer bonding, substrates are bonded to each other after surface treatment by chemical agents or fast atom beams. Hence, direct wafer bonding is assumed to enable us to fabricate heterojunctions easily. However, high-temperature annealing is necessary to form junctions in wafer-fused bonding.[16,17] Such a high-temperature process might cause the degradation of crystal qualities due to the evaporation of arsenic atoms or mechanical defects due to the difference between the thermal expansion coefficients of bonded substrates. In SAB, substrate surfaces are activated by the fast atom beams of Ar prior to bonding without heating. These methods have widely been used for fabricating various junctions, such as Si/Si,[18,19] Si/SiC,[20] GaAs/Si,[21] and InGaP/Si.[22] However, it has been reported that interface states with high densities exist at the bonding interface, which is assumed to be due to the formation of interlayers or the imperfection of the interface.[23,24]

Lian et al. fabricated GaAs/GaN p–n heterojunction diodes by wafer-fused bonding and characterized their electrical properties by capacitance–voltage (C–V) and temperature–dependent current–voltage (I–V) measurements.[17] They presumed that the band alignment was of type II. Kim et al. also reported on GaAs/GaN p–n heterojunction diodes,[3] which were fabricated by bonding GaAs and GaN substrates to each other after their surfaces were activated by the O_2 plasma. They suggested that the band alignment was of type I. Given that the electron affinities of GaAs and GaN are reportedly 4.07 and 4.1 eV, respectively, their conduction band discontinuity should be ~0 eV in the simplest model. The disagreement in the previously reported two band alignments (type I vs type II), consequently, suggests that a dipole is formed at the GaAs/GaN interface affecting the apparent band alignments. Such a dipole should likely be sensitive to the process of forming the GaAs/GaN interface. The standard model for heterointerfaces[25] predicts that the magnitude of the dipole is sensitive to the charge neutrality level (CNL)[26] of the adjacent layers. It is also notable that the band bending in each layer depends on the interface charge, or the density of interface states (D_{it}). The impacts of the interface states on the electrical properties of GaAs/GaN junctions as well as the band alignments, however, have not yet been fully understood.

We previously reported on C–V characteristics of p^+-GaAs/n-GaN junctions.[27] In this study, we fabricated p^+-GaAs/n-GaN and n^+-GaAs/n-GaN junctions by SAB. The electrical properties of the respective junctions were investigated by measuring their C–V and I–V characteristics. We analyzed the effects of charges in the interface states on the C–V characteristics of p^+-GaAs/n-GaN and n^+-GaAs/n-GaN junctions by using the CNL model. The band alignment of the GaAs/GaN interface was estimated from analysis results. Furthermore, the effective barrier heights for the two junctions were estimated using the dependences of their I–V characteristics on the ambient temperature.

2. Experimental methods

We epitaxially grew p^+- and n^+-GaAs layers on p-GaAs(100)

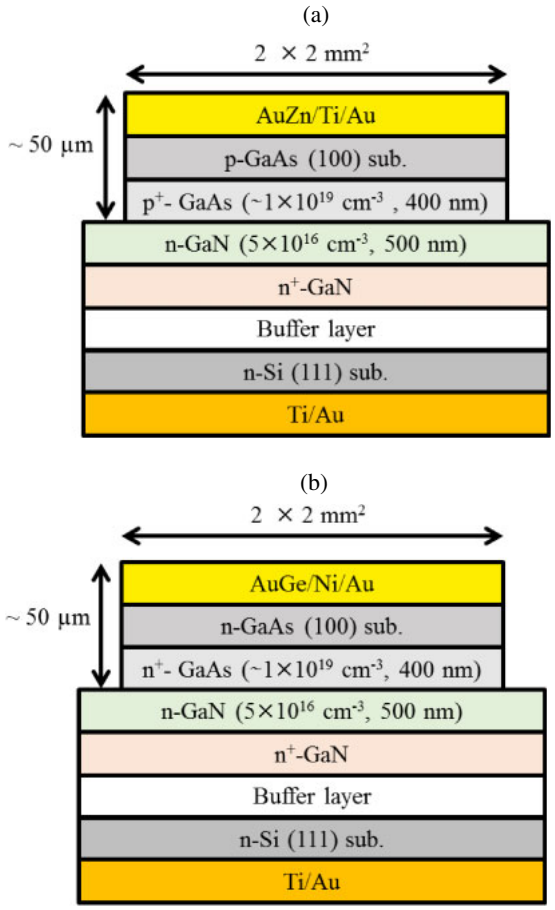

Fig. 1. (Color online) Schematic cross sections of GaAs/GaN junctions: (a) p^+-GaAs/n-GaN and (b) n^+-GaAs/n-GaN.

and n-GaAs(100) substrates, respectively. The nominal doping concentration and thickness of p^+- and n^+-GaAs layers were $\sim 1 \times 10^{19}\,cm^{-3}$ and 500 nm, respectively. We also prepared an n-GaAs layer epitaxially grown on an n-Si(111) substrate via a buffer layer. The doping concentration and thickness of the n-GaN layer were nominally $5 \times 10^{16}\,cm^{-3}$ and 400 nm, respectively.

We first formed $2 \times 2\,mm^2$ mesas on each of the p^+- and n^+-GaAs layers by using a dicer. The height of the mesas was approximately 50 μm. We bonded each of the GaAs substrates to the n-GaN epitaxial substrates by SAB to fabricate p^+-GaAs/n-GaN and n^+-GaAs/n-GaN junctions. After bonding, GaAs substrates were ground to form $2 \times 2\,mm^2$ GaAs/GaN junctions. Contacts on the back side of p-GaAs substrates were formed by evaporating AuZn/Ti/Au multilayers. Those on the back side of n-GaAs substrates were fabricated by evaporating AuGe/Ni/Au multilayers. Both the p^+-GaAs/n-GaN and n^+-GaAs/n-GaN junctions were annealed at 400 °C for 60 s in N_2 gas ambient. Then, we evaporated Ti/Au multilayers on the back side of n-Si substrates. The area and thickness of the mesas were $2 \times 2\,mm^2$ and ~50 μm, respectively. The schematic cross sections of the p^+-GaAs/n-GaN and n^+-GaAs/n-GaN junctions are shown in Fig. 1. Their *I–V* characteristics were measured with n-GaN grounded at various ambient temperatures between 20 and 200 °C by using the ADCMT 6242 source measurement unit. *C–V* characteristics were measured with n-GaN grounded at room temperature by using the Agilent E4980A precision impedance analyzer.

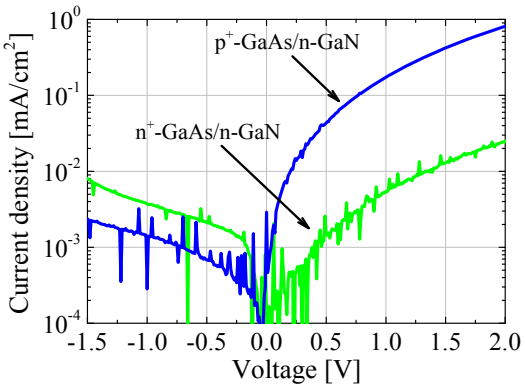

Fig. 2. (Color online) *I–V* characteristics of SAB-based GaAs/GaN junctions measured at room temperature.

3. Results

The *I–V* characteristics of p^+-GaAs/n-GaN and n^+-GaAs/n-GaN junctions are shown in Fig. 2. The curve of p^+-GaAs/n-GaN revealed rectifying properties similarly to those of conventional p–n junctions. Although the *I–V* curve of the n^+-GaAs/n-GaN heterojunction measured at room temperature showed high leakage currents, the *I–V* characteristics measured at −50 °C revealed rectifying properties similarly to that of conventional Schottky junctions (not shown here). The reverse-bias current at low reverse bias voltages was sufficiently low to measure *C–V* characteristics. In addition, we found (not depicted) that the current for forward-bias voltages higher than 8.0 V was almost proportional to the bias voltages in both *I–V* characteristics, suggesting that the conduction properties in this voltage region were dominated by the parasitic resistance. We estimated the parasitic resistance to be 0.18 and 5.3 kΩ cm² for the p^+–n and n^+–n junctions, respectively, from the slope of the curve between 9 and 10 V. The obtained parasitic resistances, which were larger than those in previous report,[3)] are likely due to the high resistivity in buffer layers between the GaN layers and the Si substrates.

The *I–V* characteristics of p^+-GaAs/n-GaN and n^+-GaAs/n-GaN junctions measured at various temperatures are shown in Figs. 3(a) and 3(b), respectively. The current increased with the bias voltage and temperature in each junction. By extrapolating the current density of each curve to +0 V, we extracted the saturation current density (J_0) at each temperature. The insets show relationships between the saturation current density divided by the square of the ambient temperature, J_0/T^2, and q/kT. The slope indicates the barrier heights at bonding interfaces. We fitted each relationship between $\ln(J_0/T^2)$ and q/kT to a straight line to estimate the barrier heights. The results of fitting are also shown in the insets of Figs. 3(a) and 3(b). Given that each relationship was separated into a high-temperature part with a large slope and a low-temperature part with a small slope, two barrier heights were likely to manifest themselves. The barrier heights for the low-temperature parts were 8 and 19 meV for the p^+-GaAs/n-GaN and n^+-GaAs/n-GaN junctions, respectively.

Figure 4 shows the $1/C^2$–*V* characteristics of two junctions measured at a frequency of 2 MHz. Using the slopes of $1/C^2$–*V* characteristics, the donor concentration of

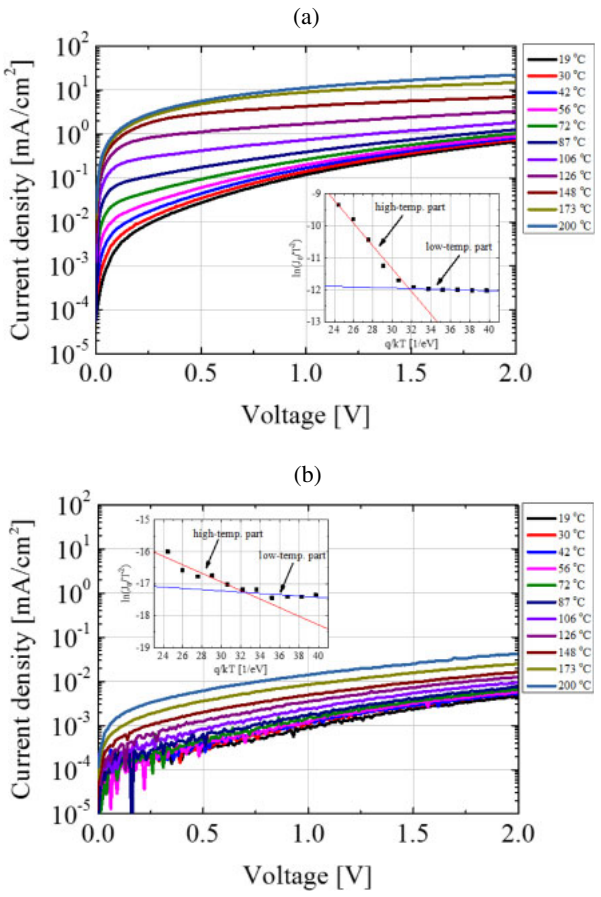

Fig. 3. (Color online) Temperature dependences of the *I–V* characteristics of (a) p$^+$-GaAs/n-GaN and (b) n$^+$-GaAs/n-GaN junctions. The inset shows relationships between the saturation current density divided by the square of the ambient temperature, J_0/T^2, and q/kT.

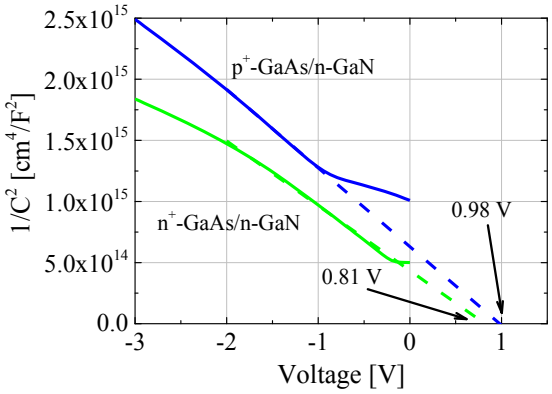

Fig. 4. (Color online) *C–V* characteristics of p$^+$-GaAs/n-GaN and n$^+$-GaAs/n-GaN junctions measured at room temperature and a frequency of 2 MHz.

the n-GaN epitaxial layer was estimated to be approximately $2.5 \times 10^{16}\,\mathrm{cm}^{-3}$ for the p$^+$-GaAs/n-GaN junction and $3.0 \times 10^{16}\,\mathrm{cm}^{-3}$ for the n$^+$-GaAs/n-GaN junction, which was close to the nominal doping concentration of the n-GaN layer ($5 \times 10^{16}\,\mathrm{cm}^{-3}$). Although a slight warp was observed in the characteristics, we extracted the flat-band voltage by linearly extrapolating $1/C^2$ to zero. The flat-band voltage was found to be 0.98 and 0.81 V for p$^+$-GaAs/n-GaN and n$^+$-GaAs/n-GaN junctions, respectively.

The difference in flat-band voltage between p$^+$-GaAs/n-GaN and n$^+$-GaAs/n-GaN junctions (ΔV_F) was, consequently, 0.17 V. This value is much smaller than that predicted using the crudest model of the band structures of heterojunctions, which gives

$$\Delta V_\mathrm{F} = \frac{1}{q}(E_\mathrm{g,GaAs} + \delta_\mathrm{p\text{-}GaAs} + \delta_\mathrm{n\text{-}GaAs}) \approx \frac{1}{q}E_\mathrm{g,GaAs} = 1.42\,\mathrm{V}. \quad (1)$$

Note that q is the elementary charge, $E_\mathrm{g,GaAs}$ is the band-gap energy of GaAs, and $\delta_\mathrm{p\text{-}GaAs}$ and $\delta_\mathrm{n\text{-}GaAs}$ refer to the positions of the Fermi level relative to the valence band maximum in p$^+$-GaAs and to the conduction band maximum in n$^+$-GaAs, respectively.

4. Discussion

The discrepancy in ΔV_F between the measurements and the prediction using the crudest model suggested that interface states with high densities were formed at the bonding interfaces and that the Fermi level was pinned. We analyzed the effects of the interface charges on the *C–V* characteristics of p$^+$-GaAs/n-GaN and n$^+$-GaAs/n-GaN junctions by using the CNL model. Here, we assumed the following: (1) The carrier concentrations of the GaAs layers are sufficiently high and their depletion regions are very thin. Consequently, the carriers trapped in the interface states are in thermal equilibrium with those in the GaAs layers, i.e., the Fermi level at the interface coincides with that in the GaAs layers irrespective of bias voltage. (2) The interface states are uniformly distributed in the overlap of band gaps of GaAs and GaN layers. Thereby, their density (D_it) is independent of their energy. (3) The distribution of charges in the GaAs layers is locally determined by solving Poisson's equation, and the distribution of charges in the GaN layer is estimated by depletion layer approximation and the space charge in the depletion layer. (4) The sum of charges in the entire junctions is zero.[28] (5) The CNL of the GaAs side coincides with that of the GaN side, i.e., surface pinning occurs. The CNL of the GaAs side is observed at 1 eV above its valence band maximum ($E_\mathrm{CNL} = 1\,\mathrm{eV}$,[29] where E_CNL is the energy of the CNL measured from the valence band edge of GaAs).

For p$^+$-GaAs/n-GaN junctions, the density of charges at interface states (Q_it) can be expressed as

$$Q_\mathrm{it} = qD_\mathrm{it}\int_0^{E_\mathrm{CNL}}[1 - f(E)]\,dE - qD_\mathrm{it}\int_{E_\mathrm{CNL}}^{E_\mathrm{g,GaAs}} f(E)\,dE. \quad (2)$$

The Fermi distribution function $f(E)$ is expressed as

$$f(E) = \frac{1}{\exp\left(\dfrac{E - E_\mathrm{f,GaAs}}{kT}\right) + 1}, \quad (3)$$

where $E_\mathrm{f,GaAs}$ is the Fermi level of the p$^+$-GaAs layer, k is the Boltzmann constant, and T is the temperature. Given the surface potential of the p$^+$-GaAs layer (φ_s), the charge density of the p$^+$-GaAs layer ($Q_\mathrm{p\text{-}GaAs}$) is expressed as

$$Q_\mathrm{p\text{-}GaAs} = -\left(4n_\mathrm{i}\varepsilon q\left\{\frac{kT}{q}\left[\cosh\left(\frac{q(\varphi_\mathrm{s} + \varphi_\mathrm{B})}{kT}\right) - \cosh\left(\frac{q\varphi_\mathrm{B}}{kT}\right)\right] - \varphi_\mathrm{s}\sinh\left(\frac{q\varphi_\mathrm{B}}{kT}\right)\right\}\right)^{1/2} \quad (4)$$

by solving Poisson's equation. In this expression, n_i is the intrinsic carrier, ε is the dielectric constant, and φ_B is the bulk

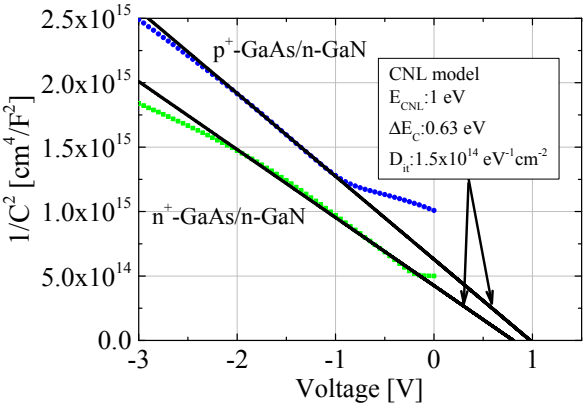

Fig. 5. (Color online) Calculated *C–V* characteristics of GaAs/GaN junctions.

potential of GaAs. The charge density of the n-GaN layer ($Q_{\text{n-GaN}}$) is obtained as

$$Q_{\text{n-GaN}} = -(Q_{\text{p-GaAs}} + Q_{\text{it}}) \tag{5}$$

to define the bias voltage. Thus, the relationship between capacitance and bias voltage is numerically calculated by gradually changing φ_s. The *C–V* characteristics of the n$^+$-GaAs/n-GaN junctions are obtained in similar manners. We formed those equations about $Q_{\text{n-GaN}}$ [Eq. (5)] for p$^+$-GaAs/n-GaN and n$^+$-GaAs/n-GaN junctions. We obtained D_{it} and ΔE_{C} by simultaneously solving these two equations. We found that the calculated $1/C^2$–V characteristics obtained by using $D_{\text{it}} = 1.5 \times 10^{14}\,\text{cm}^{-2}\,\text{eV}^{-1}$ and $\Delta E_{\text{C}} = 0.63\,\text{eV}$ are in good agreement with the experimental results for both the p$^+$–n and n$^+$–n junctions, as shown in Fig. 5. We also found that $D_{\text{it}} = 1.5 \times 10^{14}\,\text{cm}^{-2}\,\text{eV}^{-1}$, which should be attributed to the irradiation of Ar beams in the SAB process, is as large as those previously reported for GaAs Schottky diodes.[30,31]

Based on E_{CNL}, D_{it}, and ΔE_{C} values, the energy band alignments for p$^+$-GaAs/n-GaN and n$^+$-GaAs/n-GaN junctions in the thermal equilibrium are shown in Figs. 6(a) and 6(b), respectively. The band alignment revealed type I features, which qualitatively agreed with a previous report for GaAs/GaN junctions that were grown by molecular beam epitaxy.[11] We confirmed that the type I features were obtained by calculation using other E_{CNL} values such as 0.5 eV.[26] Consequently, the band alignment of GaAs/GaN interfaces obtained by the SAB is likely to reveal type I features irrespective of the ambiguity in E_{CNL}.

As the temperature increased, the potential barriers became larger, suggesting that the thermionic emission was dominant at higher temperatures. The heights of potential barriers that carriers should overcome at room temperature are 10–20 meV for both the p$^+$-GaAs/n-GaN and n$^+$-GaAs/n-GaN junctions as is shown in the insets of Figs. 3(a) and 3(b), respectively. This suggests that the dominant mechanism of carrier transport across the interfaces is tunneling through the interface states for both junctions. The comparatively large reverse-bias currents observed for the two junctions support this hypothesis. The large difference in parasitic resistance between the p$^+$-GaAs/n-GaN and n$^+$-GaAs/n-GaN junctions, consequently, might be related to the tunneling probabilities of the respective junctions.

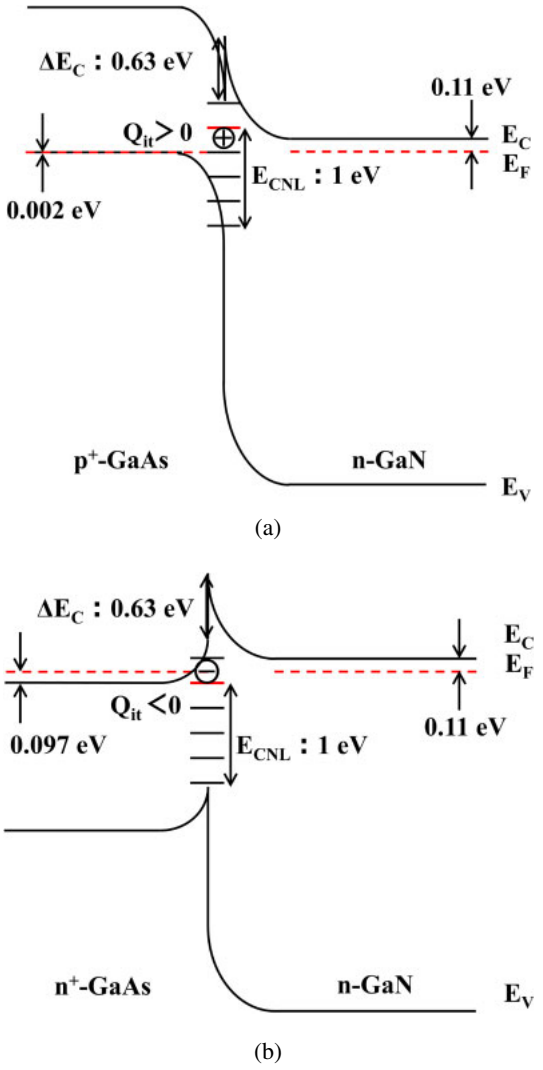

Fig. 6. (Color online) Energy band alignments for (a) p$^+$-GaAs/n-GaN and (b) n$^+$-GaAs/n-GaN junctions.

From the practical viewpoint, D_{it} such as $\sim 10^{14}\,\text{cm}^{-2}\,\text{eV}^{-1}$ must be lowered. In the analogy to Si/Si junctions,[23] D_{it} is assumed to be lowered by long-period post-bonding annealing. The annealing in the atmosphere in combination with reverse-bias voltages might be useful.[32] Otherwise, applications with small impacts of interface states such as reversely biased GaAs/GaN junctions should be explored. The type I band alignment suggests that SAB-based GaAs/GaN junctions are potentially applicable to high-voltage devices since high reverse-bias voltages can be applied when ideal interfaces are achieved.

5. Conclusions

We fabricated p$^+$-GaAs/n-GaN and n$^+$-GaAs/n-GaN junctions by surface-activated bonding and examined their electrical properties by measuring capacitance–voltage and current–voltage characteristics. The flat-band voltages of respective junctions deduced from the capacitance–voltage characteristics at 2 MHz were similar (0.98 V: p$^+$-GaAs/n-GaN; 0.81 V: n$^+$-GaAs/n-GaN), which was attributed to the pinning of the Fermi level at the bonding interface. The effects of the interface state charges on the *C–V* characteristics of p$^+$-GaAs/n-GaN and n$^+$-GaAs/n-GaN junctions were analyzed using the CNL model. The modeled *C–V*

characteristics were in agreement with the experimental results when the interface state density and conduction band discontinuity were assumed to be $1.5 \times 10^{14}\,\mathrm{cm^{-2}\,eV^{-1}}$ and 0.63 eV, respectively. The band alignment of GaAs/GaN junctions extracted using this model suggested type I features. The dependences of *I–V* characteristics on the ambient temperature were analyzed; thus, tunneling through interface states with such a high density was identified as the dominant mechanism of carrier transport across the interfaces of both junctions. Consequently, the difference in parasitic resistance between the p^+-GaAs/n-GaN and n^+-GaAs/n-GaN junctions might be related to the tunneling probabilities of the respective junctions.

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