Effects of annealing on electrical properties of Si/Si junctions by surface-activated bonding



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# Effects of annealing on electrical properties of Si/Si junctions by surface-activated bonding

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Effects of annealing on surface-activated bonding (SAB)-based Si/Si junctions were investigated by transmission electron microscopy (TEM) observations and current–voltage ($I$–$V$) measurements. We observed an amorphous-like layer at the bonding interface, which was recrystallized by annealing. We extracted the potential barrier heights at Si/Si interfaces annealed at different temperatures from the results of $I$–$V$ measurements at various ambient temperatures. For p-Si/p-Si junctions, the barrier height increased as the annealing temperature increased from 200 to 400 °C and decreased from 400 to 1000 °C. For n-Si/n-Si junctions, the barrier height increased as the annealing temperature increased from 200 to 600 °C and decreased from 600 to 1000 °C. By using the charge neutral level (CNL) model, we estimated the energy of CNL, $E_{CNL}$, and the density of interface states, $D_{it}$, at each annealing temperature. $D_{it}$ decreased as the annealing temperature increased from 400 to 1000 °C. $E_{CNL}$ showed values larger than the reported ones. 

## 1. Introduction

Heterojunctions composed of dissimilar semiconductor materials are widely used to fabricate high-performance electrical and optical devices. Given that the epitaxial growth of semiconductor layers with different crystal structures, thermal expansion coefficients, and lattice constants is, in general, difficult, the possibility of applying direct wafer bonding to prepare such heterojunctions has been explored.[1)] Actually, direct wafer bonding has been employed to fabricate, for example, GaAs/Si[2,3)] GaAs/InP,[4)] InP/Si,[5)] and Si/$SiO_2$[6)] junctions. In this method, however, annealing at a high temperature (typically ~600 °C) is necessary during or after bonding to achieve sufficient bonding strength.[7)] This means that the bonded substrates with thicknesses of several hundred microns should be annealed at high temperatures. In addition, the electrical characteristics of bonding interfaces depend on chemical treatments of surfaces before bonding.[8)] It is consequently assumed that the applicability of conventional direct wafer bonding as a method for fabricating heterojunctions is limited.

By surface-activated bonding (SAB),[9–11)] in which samples are brought into contact in a vacuum chamber after oxidized layers on their surfaces are etched off by Ar fast atom beam (FAB) irradiation, substrates are bonded without intentionally heating them. It was reported that the strength of SAB was greater than that of direct bonding.[12)] In addition, it is assumed that the electrical properties of the interfaces obtained by SAB are less sensitive to prebonding chemical treatments than those of interfaces obtained by direct wafer bonding since the surfaces of SAB samples are processed through Ar FAB irradiation. Therefore, SAB is attractive for fabricating various devices with heterojunctions, such as tandem solar cells.[13)]

The Ar FAB irradiation of surfaces, however, reportedly leads to the formation of an amorphous-like layer at the bonding interface.[14)] The interface states with high densities are assumed to be introduced through Ar FAB irradiation. Previous reports showed that the thickness of the amorphous-like layer decreased and the current–voltage ($I$–$V$) characteristics changed with annealing.[15,16)] In this work, we fabricated Si/Si junctions and annealed them at different temperatures. We observed the interface by transmission electron microscopy (TEM) and measured the $I$–$V$ characteristics of junctions. Furthermore, we discussed the correlation between the electrical properties of the interface and the annealing temperature in the framework of the charge neutral level (CNL) model.

## 2. Methods

We employed (100) p-Si and (100) n-Si substrates. The carrier concentrations of p-Si and n-Si substrates were $2.4 \times 10^{17}$ and $4.8 \times 10^{16}$ $cm^{-3}$, respectively. The surfaces of these substrates were cleaned with acetone and ethanol, and activated by Ar FAB irradiation for 180 s. The pressure was below $5 \times 10^{-6}$ Pa immediately before Ar FAB irradiation. After surface activation, the substrates were brought into contact and pressed for 60 s at 10 MPa. The temperature of the substrates was not intentionally raised while they were being bonded. These samples were annealed at different temperatures (400, 600, 800, and 1000 °C) for 10 min. Electrodes on the back of p-Si substrates were formed by evaporating Al and annealing (400 °C, 1 min) to prepare p-Si/p-Si junctions with interfaces annealed at temperatures between 400 and 1000 °C. Two more p-Si/p-Si junctions were fabricated by forming electrodes on the back of p-Si substrates and bonding them under the above conditions. Then, one of them was annealed at 200 °C for 10 min. n-Si/n-Si junctions with interfaces annealed at 200, 400, 600, 800, and 1000 °C were obtained by bonding n-Si substrates, annealing them at a various temperatures, and evaporating Ti/Au on the back of the Si substrates. All twelve samples were diced into $2 \times 2$ $mm^2$ chips. We measured their $I$–$V$ characteristics between −185 and 200 °C. We also observed the interfaces without annealing and after annealing at 1000 °C by TEM.

It was previously reported that interface states were formed at interfaces fabricated by direct bonding.[17–19)] The interface states that trap carriers are likely to produce a potential barrier and depletion layers neighboring the interface, as is schematically shown in Fig. 1. The density of electrical charges at the interface, $Q_{it}$, is described using the CNL model, in which interface states with energies lower (higher) than that of the CNL, $E_{CNL}$, are assumed to have donor like (acceptor like) features. We define $E_{CNL}$ as the separation between the CNL and the valence band edge at the interface.[20)] The Fermi level at the interface relative to $E_{CNL}$ determines $Q_{it}$, which is expressed as

 

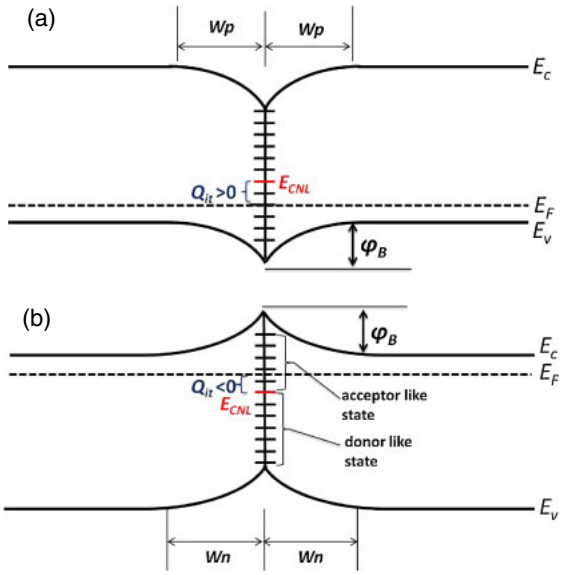


**Fig. 1.** (Color online) Schematic band diagrams of (a) p-Si/p-Si and (b) n-Si/n-Si junctions.

$$Q_{\mathrm{it,p}} = qD_{\mathrm{it}}(E_{\mathrm{CNL}} - \varphi_{\mathrm{B}} + \delta_{\mathrm{p}}), \tag{1}$$

$$Q_{\mathrm{it,n}} = qD_{\mathrm{it}}(E_{\mathrm{g}} - \varphi_{\mathrm{B}} + \delta_{\mathrm{n}} - E_{\mathrm{CNL}}), \tag{2}$$

for p-Si/p-Si and n-Si/n-Si junctions, respectively. In these expressions, "p" and "n" denote p-Si/p-Si and n-Si/n-Si junctions, respectively. $D_{\mathrm{it}}$ is the density of interface states and $\varphi_{\mathrm{B}}$ is the potential barrier height at the interface. We assume that $D_{\mathrm{it}}$ is independent of energy, i.e., the interface states are uniformly distributed in the band gap and the carriers in the interface states are degenerated. $\delta_{\mathrm{p(n)}}$ is the difference between the valence (conduction) band edge and the Fermi level. We find, from Fig. 1, that the magnitude of $Q_{\mathrm{it}}$ increases (decreases) as $E_{\mathrm{CNL}}$ increases for p-Si/p-Si (n-Si/n-Si) junctions. From the requirement that $Q_{\mathrm{it}}$ should be compensated by the charges in the depletion region, $Q_{\mathrm{it}}$ is also expressed as

$$Q_{\mathrm{it,p(n)}} = 2qN_{\mathrm{a(d)}}w_{\mathrm{p(n)}}, \tag{3}$$

where $N_{\mathrm{a(d)}}$ is the concentration of acceptors (donors) in p-Si (n-Si) substrates and $w_{\mathrm{p(n)}}$ is the thickness of their depletion region. From Poisson's equation, the barrier height is expressed as

$$\varphi_{\mathrm{B}} = \frac{q^2 N_{\mathrm{a(d)}} w_{\mathrm{p(n)}}^2}{2\varepsilon} = \frac{Q_{\mathrm{it,p(n)}}^2}{8\varepsilon N_{\mathrm{a(d)}}}. \tag{4}$$

Here, $\varepsilon$ is the dielectric constant of Si. This equation indicates that $\varphi_{\mathrm{B}}$ depends on $Q_{\mathrm{it}}$ and $N_{\mathrm{a(d)}}$.

The current of junctions with a potential barrier is modeled using the thermionic emission model.[21] In this model, only the carriers with energies greater than the potential barrier can contribute to the current. By assuming that the barrier height of one side of the junction changes to $\varphi_{\mathrm{B}} + qV$ while the barrier height of the other side remains $\varphi_{\mathrm{B}}$ when a bias voltage $V$ is applied to the junction, the net current across the junction, $I_{\mathrm{th,p(n)}}$, is described as

$$I_{\mathrm{th,p(n)}} = A^*_{\mathrm{p(n)}} T^2 \exp\left(-\frac{\varphi_{\mathrm{B}} - \delta_{\mathrm{p(n)}}}{k_{\mathrm{B}}T}\right)\left[1 - \exp\left(-\frac{qV}{k_{\mathrm{B}}T}\right)\right], \tag{5}$$

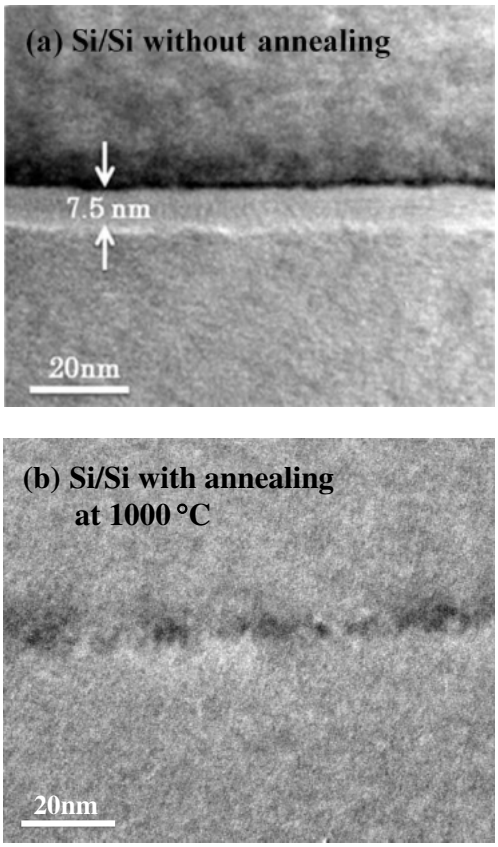


**Fig. 2.** (Color online) TEM images of Si/Si bonding interfaces (a) without and (b) with annealing at 1000 °C for 10 min.

where $A^*_{\mathrm{p(n)}}$ is the Richardson constant, $k_{\mathrm{B}}$ is the Boltzmann constant, and $T$ is the ambient temperature. Providing that $qV \ll kT$, the following approximation holds

$$1 - \exp\left(-\frac{qV}{k_{\mathrm{B}}T}\right) \cong \frac{qV}{k_{\mathrm{B}}T}. \tag{6}$$

Using the two equations, we obtain

$$\ln\left(\frac{G}{T}\right) = \ln\left(\frac{\lim_{V\to 0}\frac{\partial I_{\mathrm{th}}}{\partial V}}{T}\right) = \ln G_0 - \frac{\varphi_{\mathrm{B}} - \delta_{\mathrm{p(n)}}}{k_{\mathrm{B}}T}. \tag{7}$$

Here, $G$ is the conductance across the junction at the zero-bias-voltage limit and $G_0 = qA^*_{\mathrm{p(n)}}/k_{\mathrm{B}}$. We extract $\varphi_{\mathrm{B}}$ by fitting the measured relationship between $\ln(G/T)$ and $(1/T)$ to Eq. (7).

## 3. Results and discussion

### 3.1 Results

Figure 2(a) shows the cross sectional TEM image of the Si/Si bonding interface without annealing. No interfacial voids or fractures were found at the nanometer scale. In this figure, an amorphous-like layer with a thickness of 7.5 nm was observed at the interface. This layer is attributed to surface damage caused by Ar FAB irradiation.[14] In contrast, this layer was not observed after annealing at 1000 °C, as is shown in Fig. 2(b). It is assumed that the recrystallization of the amorphous-like layer occurred with annealing. This result is consistent with that previously reported.[14,16]

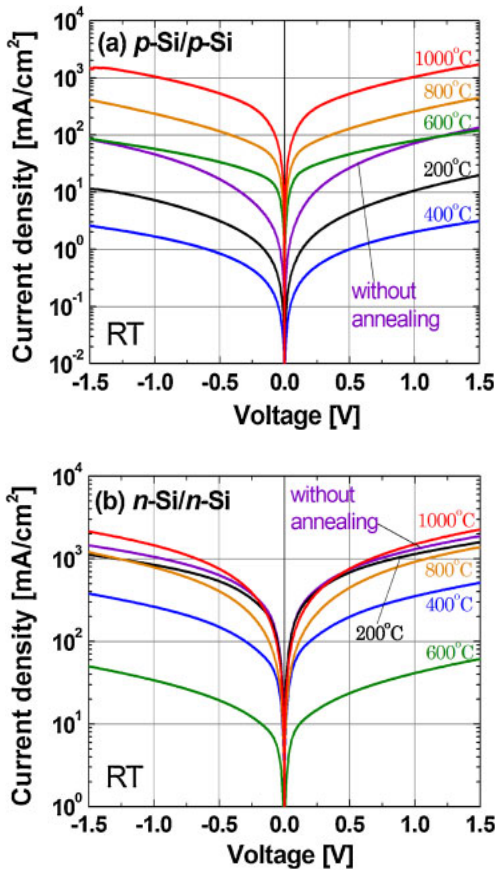


**Fig. 3.** (Color online) *I–V* characteristics of (a) p-Si/p-Si and (b) n-Si/n-Si junctions without and with annealing at 200, 400, 600, 800, and 1000 °C for 10 min.

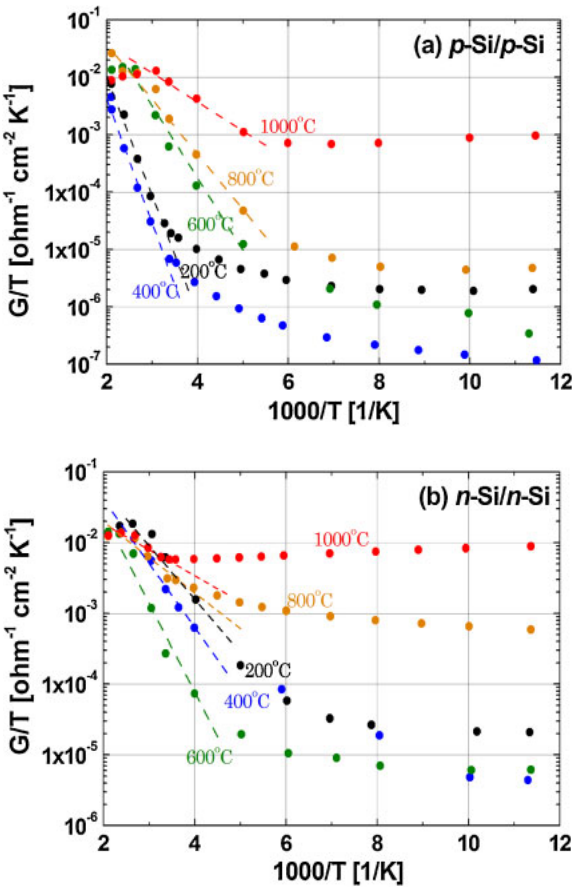


**Fig. 4.** (Color online) Relationship between the conductance at zero-bias-voltage limit and the temperature for annealed (a) p-Si/p-Si and (b) n-Si/n-Si junctions.

Figure 3(a) shows the *I–V* characteristics of p-Si/p-Si junctions with and without annealing measured at room temperature. The results for the n-Si/n-Si junctions are shown in Fig. 3(b). The *I–V* characteristics in the respective figures are approximately symmetric. As is shown in Fig. 3(a), the current density of p-Si/p-Si junctions decreased as the annealing temperature increased up to 400 °C and then increased as the annealing temperature increased from 400 to 1000 °C. The current density of n-Si/n-Si junctions decreased as the annealing temperature increased up to 600 °C and then increased as the annealing temperature increased from 600 to 1000 °C. The decrease in current owing to annealing at temperatures up to 600 °C, in which the contact resistance was assumed to play a major role,[16] has been reported in the literature.

The relationship between $\ln(G/T)$ and $(1/T)$ for the annealed p-Si/p-Si and n-Si/n-Si junctions is shown in Figs. 4(a) and 4(b), respectively. The results of fitting using Eq. (7) are also shown by dashed lines in these figures. A good fit was obtained for the respective curves in comparatively high temperature ranges, suggesting that the current due to the thermionic emission was dominant at higher temperatures. The relationship between the extracted $\varphi_B$ and the annealing temperature is shown in Fig. 5. The $\varphi_B$ of p-Si/p-Si junctions increased as the annealing temperature increased from 200 to 400 °C and decreased as the annealing temperatures increased from 400 to 1000 °C. The $\varphi_B$ of n-Si/n-Si junctions increased as the annealing temperature increased up to 600 °C and decreased as the annealing temperature increased further.

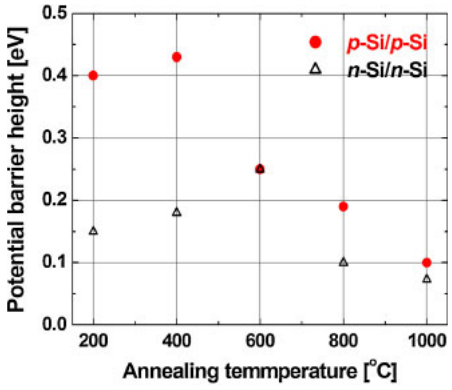


**Fig. 5.** (Color online) Relationship between the potential barrier height at Si/Si interface and annealing temperature.

These $\varphi_B$ trends are consistent with the variation in current owing to annealing, as is seen in Figs. 3(a) and 3(b).

### 3.2 Discussion

We estimated $Q_{it}$ of the respective junctions from their $\varphi_B$ using Eq. (4). Then, we obtained the relationship between $D_{it}$ and $E_{CNL}$ for the p-Si/p-Si and n-Si/n-Si junctions annealed at the respective temperature using Eqs. (1) and (2). The obtained curves for junctions annealed at 200, 400, 600, 800, and 1000 °C are shown in Figs. 6(a)–6(e), respectively. Here

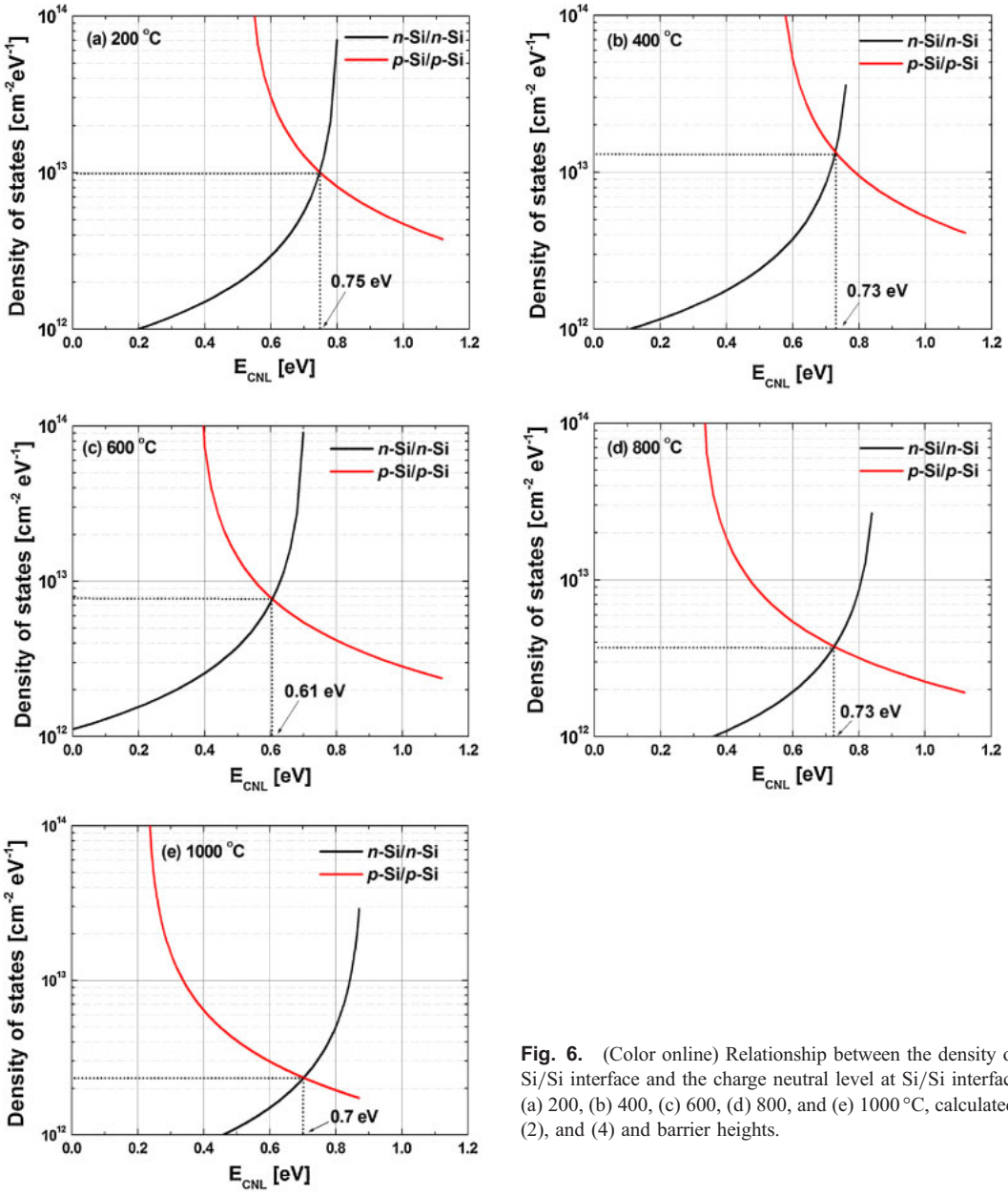


**Fig. 6.** (Color online) Relationship between the density of states at the Si/Si interface and the charge neutral level at Si/Si interfaces annealed at (a) 200, (b) 400, (c) 600, (d) 800, and (e) 1000 °C, calculated using Eqs. (1), (2), and (4) and barrier heights.

we assume that $D_{it}$ and $E_{CNL}$ depend on the conditions of surface activation and annealing and are not sensitive to the polarity of the substrates. This means that $D_{it}$ and $E_{CNL}$ in the p-Si/p-Si junction annealed at, for example, 400 °C are the same as those in the n-Si/n-Si junction annealed at 400 °C. On the basis of this assumption, $D_{it}$ and $E_{CNL}$ are given by the intersection of the two curves in each figure.

The estimated $E_{CNL}$ and $D_{it}$ are shown in Fig. 7. Although the data are largely scattered, we find that $E_{CNL}$ decreases as the annealing temperature increases. We also find that the estimated $E_{CNL}$, 0.61–0.75 eV above the valence band edge of Si, is higher than that previously reported, which was approximately one-third of the band gap (0.36 eV).[20] It was reported that Schottky barrier heights increased in p-Si Schottky diodes and decreased in n-Si Schottky diodes with the implantation of Ar ions.[22,23] It was also reported that the barrier heights in the p-Si (n-Si) Schottky diodes decreased (increased) with annealing after the implantation of Ar ions.[24] These results were explained by the scheme in which donor like defects were generated and $E_{CNL}$ was increased by

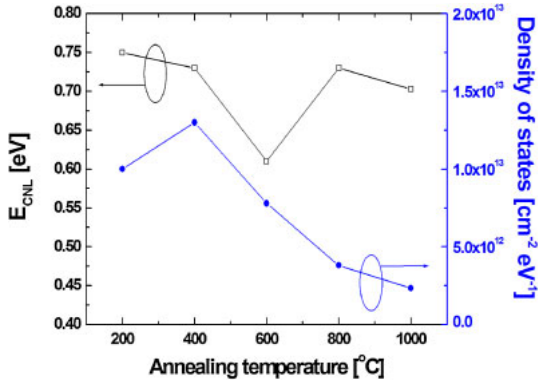


**Fig. 7.** (Color online) Dependences of $D_{it}$ and $E_{CNL}$ on the annealing temperature.

Ar implantation. It was also assumed that the damage due to the implantation was recovered by annealing and $E_{CNL}$ was lowered. The $E_{CNL}$ values higher than 0.36 eV and their

variation due to annealing observed in the present work might be explained by a similar mechanism. We also find that $D_{it}$ roughly decreases as the annealing temperature increases, which is assumed to be consistent with the results of TEM observation that the amorphous-like layer in the vicinity of the interface was recrystallized by the annealing [Figs. 2(a) and 2(b)].

Using Eqs. (1) and (2), the lowering of $E_{CNL}$ is considered to reduce $\varphi_B$ in the p-Si/p-Si junctions and increase it in the n-Si/n-Si junctions. The decrease in $D_{it}$ should bring about the decrease in $\varphi_B$ both in the p-Si/p-Si and n-Si/n-Si junctions. The changes in $E_{CNL}$ and $D_{it}$ are consequently assumed to additively reduce $\varphi_B$ in the p-Si/p-Si junctions. The changes in the two parameters might contradictively act to realize the variation in $\varphi_B$ in the n-Si/n-Si junctions, which increased up to 600 °C and decreased for higher temperatures.

Given that $\varphi_B$, $E_{CNL}$, and $D_{it}$ are ~0.2 eV, ~0.7 eV, and $\sim 10^{13}\,cm^{-2}\,eV^{-1}$, respectively, the depletion layer thickness in the n-Si/n-Si junctions is estimated to be $\sim 10^{-7}$ cm at a doping concentration of $10^{19}\,cm^{-3}$ using Eqs. (2) and (3). If interfaces with such low barrier heights and narrow depletion layers are obtained in junctions made of dissimilar materials such as Si/GaAs systems, the resistance across the bonding interface does not severely affect the characteristics of the tandem cells obtained by bonding. The results of the present work suggest that the resistance across the interfaces is lowered by annealing them. Bonded interfaces with lower densities of interface states are likely to be obtained by optimizing the conditions of Ar FAB irradiation.

## 4. Conclusions

We fabricated p-Si/p-Si and n-Si/n-Si junctions by SAB and annealed them at different temperatures. We then characterized them by TEM observations and *I–V* measurements. We observed an amorphous-like layer at the bonding interface, which was recrystallized by annealing. We extracted the potential barrier height $\varphi_B$ at annealed Si/Si interfaces from the dependences of their *I–V* characteristics on the ambient temperature. For p-Si/p-Si junctions, $\varphi_B$ increased as the annealing temperature increased from 200 to 400 °C and decreased from 400 to 1000 °C. For n-Si/n-Si junctions, $\varphi_B$ increased as the annealing temperature increased from 200 to 600 °C and decreased from 600 to 1000 °C. Using the charge neutral level (CNL) model, we estimated the energy of CNL, $E_{CNL}$, and the density of interface states $D_{it}$ at each annealing temperature. One explanation was given for the relationships among $E_{CNL}$, $D_{it}$, and $\varphi_B$.

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