Plane-view transmission electron microscopy of Si/GaAs interfaces fabricated by surface-activated bonding at room temperature

Yutaka Ohno[1], Hideto Yoshida[2], Seiji Takeda[2], Liang Jianbo[3], and Naoteru Shigekawa[3]

[1] *Institute for Materials Research (IMR), Tohoku University, Katahira 2-1-1, Aoba, Sendai 980-8577, Japan*
[2] *The Institute of Scientific and Industrial Research (ISIR), Osaka University, Mihogaoka 8-1, Ibaraki, Osaka 567-0047, Japan*
[3] *Graduate School of Engineering, Osaka-City University, Sugimoto 3-3-138, Sumiyoshi, Osaka 558-8585, Japan*

***Abstract*— Si/GaAs interfaces fabricated by surface-activated bonding at room temperature were examined by plane-view transmission electron microscopy. It was hypothesized that the interface resistance would be originated from surface defects on the Si and GaAs substrates introduced during the bonding process.**

I. Introduction And Background

Tandem cells consisting of Si and III-V compounds are one of the promising candidates for next-generation high-performance solar cells. However, Si/III-V interfaces free from structural defects, by which a current flow is not disturbed, have been hardly fabricated by epitaxial deposition because of the differences in crystal lattice and thermal expansion coefficient. Recently, a surface-activated bonding (SAB) method at room temperature, in which surfaces of substrates are activated by the fast atom beams of argon prior to bonding, is applied to form Si/GaAs interfaces with a low interface resistance,[1] and InGaP/GaAs/Si hybrid triple-junction cells with a conversion efficiency above 26% are fabricated.[2] The interface resistance varies depending on the SAB condition of argon atom irradiation and post-growth annealing,[1] even though the origin of the resistance is unclear. Accordingly, a comprehensive knowledge of the electrical property at the interfaces depending on their atomistic structure is indispensable to establish the fabrication processes of high-efficiency tandem cells by optimizing the interface structure.

II. Results

Interfaces of p-Si/n-GaAs were fabricated under a SAB condition at room temperature,[1] with the substrates of B-doped (001) p-Si (with a carrier concentration of $2x10^{14}$ cm^{-3}) and Si-doped n-GaAs ($2x10^{16}$ cm^{-3}) which was 5° off from (001) towards [110]. Parts of the SAB interfaces were then annealed at 473 K or 673 K for 1 minute. Thin foils with a SAB interface were prepared by mechano-chemical etching, without ion milling, so as not to introduce defects on the interface, and they were determined by transmission electron microscopy (TEM).

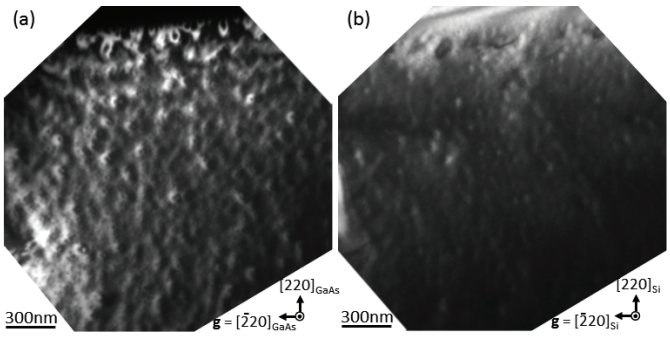

Fig. 1. Plane-view TEM images of a Si/GaAs interface fabricated by SAB at room temperature, taken with the reflections of **g** = [220] (a) for GaAs and (b) for Si. We can select those reflections separately due to an off-angle of 5° on the (001) surface of the GaAs substrate.

It has been reported that an amorphous layer is formed at an as-bonded SAB interface.[1] The layer consisted of a partially-amorphized Si layer (about 3 nm thick) on the Si substrate and a thin Si oxide layer (less than about 0.5 nm thick) existing at the GaAs/amorphous interface. A surface of the Si substrate was, therefore, amorphized during argon atom irradiation for surface activation, and the surface of the amorphous layer was slightly oxidized during the subsequent bonding process. Besides, a surface on the GaAs substrate was kept in the crystalline phase during the SAB process. Plane-view TEM of the SAB interface (i.e., TEM observed normal to the interface) revealed that there was no structural defects expanding along the interface, such as cracks and misfit dislocations, resulting in a low resistance at the SAB interface.[1] The Si/amorphous interface was rather smooth, although the GaAs/amorphous interface was strained presumably due to dimples (about 5 nm in size) introduced on the GaAs surface by argon atom irradiation, dumps (about 20 nm in size) related to threading dislocations in GaAs, and Si oxides on the Si substrate (Fig. 1). Those strains were reduced by annealing according to the recrystallization of the Si amorphous layer, and this would result in the reduction of the resistance at the SAB interface.[1] It is therefore hypothesized that the interface resistance would be originated from the defects at the GaAs/amorphous interface, and therefore the resistance might be reduced further by smoothing a surface on the GaAs substrate and/or removing the Si oxide layer on the Si substrate, via optimization of the SAB condition.

Acknowledgment

A part of this work was supported by "Research and Development of ultra-high efficiency and low-cost III–V compound semiconductor solar cell modules (High efficiency and low-cost III–V/Si tandem)" project of NEDO, by JSPS KAKENHI Grant No. 15H03535 (2015-2018), and by "Network Joint Research Center for Materials and Devices: Dynamic Alliance for Open Innovation Bridging Human, Environment and Materials" in ISIR, Osaka University.

References

[1] J. Liang, L. Chai, S. Nishida, M. Morimoto, and N. Shigekawa, Jpn. J. Appl. Phys. 54 (2015) 030211
[2] N. Shigekawa, J. Liang, R. Onitsuka, T. Agui, H. Juso, and T. Takamoto, Jpn. J. Appl. Phys. 54 (2015) 08KE03.