1 Fabrication of p^+-Si/p-diamond heterojunction diodes and effects of thermal annealing on their
2 electrical properties

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13 Keywords: diamond, surface activated bonding, heterojunction diodes, electrical properties
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15 We fabricate p^+-Si/p-diamond heterojunction diodes by using surface-activated bonding and
16 examine the electrical properties of Si/diamond interfaces by measuring current-voltage and current-
17 voltage-temperature characteristics. We find that the electrical properties of heterojunction diodes are
18 improved by post-bonding annealing at temperatures up to 873 K in terms of the ideality factor and
19 reverse-bias current. Additionally, fabricated diodes also reveal thermal stability similar to that of
20 Cu/diamond Schottky diodes. The barrier height at Si/diamond bonding interfaces annealed at 873 K
21 is estimated to be 0.55 and 0.66 eV by analyzing the relationship between the saturation current
22 density and temperature and the reverse-bias characteristics at room temperature, respectively. These

values are close to that obtained by assuming that no offset is formed in the vacuum level across the Si/diamond bonding interfaces (0.36 eV).

1. Introduction

Among ultra-wide bandgap (UWBG) semiconductors such as AlN, diamond, and Ga_2O_3, diamond is the most promising material for the fabricating of high power, high temperature [1], and high radiation resistant semiconductor devices [2] because of its UWBG (5.5 eV), high breakdown field (>10 MV/cm), high bulk carrier mobility (3800 and 4500 $cm^2V^{-1}s^{-1}$ for holes and electrons, respectively) [3,4], and high displacement energy (43 eV/atom) [5]. Diamond Schottky diodes with a low switching loss [6] and a high breakdown voltage [7–9] were demonstrated. Characteristics of diodes using sputter-deposited Si:W alloy as Schottky contacts at temperatures up to 1273K were previously reported [10,11]. However, characteristics of diodes using Si:W alloy, Cu, Ag and Al as Schottky contacts reportedly degraded by annealing at 1073, 1023, 923 and 723 K [12–14], respectively. This means that the potential of diamond has not yet been fully exploited in the present Schottky diode configuration. More excellent performances of diamond-based electron devices could be achieved by replacing Schottky contact metals with semiconductors. Boron(B)-doped Si and natural single crystalline diamond (nSCD) were previously bonded by a stamp-assisted transfer printing method and annealed for 40 min at 1073 K under nitrogen ambient [15]. Then, B atoms were reportedly diffused in nSCD so that heavily B-doped nSCD was achieved. Using the same approach, pi diodes, whose intrinsic parts were made of p-type doped diamond/intrinsic diamond junctions, with Si/diamond junctions as ohmic contacts (anodes) were fabricated and their characteristics were

1 demonstrated.

2 Using surface activated bonding (SAB), in which the sample surfaces are activated by Ar fast atom
3 beams (FAB) in a high vacuum prior to bonding in low temperatures [16–18], we previously
4 fabricated Si/diamond, Cu/diamond, GaAs/diamond, and GaN/diamond heterojunctions [19-22]. We
5 also examined effects of post-bonding annealing on their nanostructural properties. Note that single-
6 crystal semiconductor materials were bonded to diamond using SAB. We also demonstrated the
7 stability of Si/diamond bonding interfaces against annealing at 1273 K [19].

8 In this work, we fabricated p^+-Si/p-diamond heterojunction diodes using SAB and examined the
9 electrical properties of Si/diamond interfaces in detail. The condition for surface activation was like
10 those in literatures [23,24]. Note that p^+-Si and p-diamond played a role of cathode and anode,
11 respectively. The current-voltage (*I-V*) and temperature-dependent *I-V* characteristics of
12 heterojunction diodes were measured before and after annealing and effects of post-bonding
13 annealing were investigated. We also compared the electric properties of p^+-Si/p-diamond
14 heterojunction diodes with those of previous reported Cu/p-diamond SBDs, which have high thermal
15 stability among diamond Schottky diodes [13].

16

17 **2. Experimental**

18 A 25 μm lightly B-doped drift layer was epitaxially grown on a heavily (~10^{20} cm^{-3}) B-doped (100)

diamond substrate. The doping concentration in the drift layer was nominally 4×10^{16} cm^{-3}. We also prepared a silicon-on-insulator (SOI) substrate that was composed of a 2.5 μm heavily (~10^{19} cm^{-3}) B-doped device layer, a 1 μm SiO_2 layer, and a Si (100) substrate. The surface of diamond drift layer was mechanically polished. The thickness of drift layer was estimated to be 21 μm after polishing. The averaged roughness (Ra) of diamond and Si surfaces were measured to be 1.0 and 0.1 nm, respectively, by an atomic force microscope. Then the device layer of SOI substrate was bonded to the drift layer of diamond using SAB and Si substrate was removed by grinding and wet etching. By subsequently removing the SiO_2 layer a p^+-Si/p-diamond heterojunction was prepared. We made p^+-Si mesas by wet etching and formed contacts on the backside of diamond substrate and the surface of Si mesas by evaporating Ti/Au and Al/Ni/Au multilayers, respectively so that p^+-Si/p-diamond heterojunction diodes were fabricated. The schematic process sequence and an optical microscope image of fabricated diodes are shown in Figs.1 and 2, respectively. We performed the sequential post-process annealing of fabricated diodes at 703 K for 30 min in the first step, at 873 K for 30 min. in the second step, and at 1073 K for 5 min. at the last step. The post-process annealing was performed in vacuum. The *I-V* characteristics at room temperature were measured for diodes before the post-process annealing and after each annealing step. The *I-V* characteristics at temperatures between 293 K and 473 K (the temperature-dependent *I-V* characteristics) were also measured for diodes annealed at 703 K and those annealed at 873 K. A source measure unit (Agilent B2902A) was used in measuring

the *I-V* and temperature-dependent *I-V* characteristics.

3. Result

The *I-V* characteristics measured at room temperature for diodes without annealing, annealed at 703 K, and at 873 K are shown in Fig. 3(a). The lower limit of current measurement (10^{-9} A, which corresponds to 2×10^{-3} mA/cm^2) is depicted by a dashed line. The respective curves revealed marked asymmetric properties, which are typical for diodes. The ideality factor for each *I-V* curve was extracted from its steepest part between -1.7 and -0.1 V. The ideality factor was estimated to be 2.62, 1.85, 1.25 and 1.3 for the unannealed diodes and the diodes annealed at 723, 873 and 1073 K, respectively. By annealing at 723 or 873 K, the magnitude of the current at 3 V decreased significantly from 1.12 to 2×10^{-3}-3×10^{-3} mA/cm^2. It increased to 7.57 mA/ cm^2 by annealing the diodes at 1073 K. The turn on voltage, which was defined as the forward-bias voltage for the current of 100 mA/cm^2, decreased from 1.75 to 1.15 V by annealing the diodes at 873 K. It drastically decreased to 0.46 V by annealing the diodes at 1073 K. The ratio of current at -3 V to that at +3 V, the rectification factor, increased from 10^4 to 10^7 by annealing at 703 or 873 K. It decreased to 10^3 by annealing at 1073 K. These parameter values for the respective annealing conditions are summarized in Table I. Reported characteristics of Cu/p-diamond Schottky diodes after annealing at 923, 973 and 1023 K also shown

1 for comparison [13].

2 The current was almost proportional to the bias voltage between -1.4 and 0 V in the unannealed

3 heterojunction diodes, which indicated that the shunt path conduction was dominant in this bias

4 voltage range. The shunt path conduction vanished by annealing diodes at 703 K. A hump was

5 observed around -1.4 V after annealing at 873 K, which suggested that Si/diamond interfaces were

6 separated into two areas with different barrier heights, as reported for Au/diamond Schottky diodes

7 after 870 K annealing [25]. The electric properties of diodes were deteriorated after annealing at 1073

8 K, which suggested B atoms of Si layer were diffused in diamond drift layer, as reported for B-

9 doped/Si nSCD heterojunctions after 1073 K annealing [15].

10 Figures 3(b) and 3(c) show the temperature-dependent *I-V* characteristics of diodes annealed at 703

11 and 873 K, respectively. It is notable that the diodes characteristics were clearly observed even at the

12 highest temperature (473 K). The turn on voltage was decreased as the ambient temperature increased.

13 In contrast, no marked increase was observed in the reverse-bias current when the ambient

14 temperature changed. We obtained the saturation current density J_s by extrapolating the steepest part

15 in each *I-V* curve for the forward bias voltages to 0 V. Figure 4 shows relationships between J_s and

16 $1/k_BT$ where k_B is the Boltzmann constant. J_s indicate electric characteristics of p^+-Si/p-diamond

17 interface. Thus, J_s can be characterized by using the thermionic emission (TE) model in contrast to

18 previous reports of pi diodes [15]. J_s corresponding to the TE model is explained by

$$J_s = A^* T^2 \exp\left(-\frac{qV_{bn}}{k_B T}\right) \quad (1)$$

Here, A^*, T, q and qV_{bn} are the Richardson constant, the ambient temperature, the elementary charge and the barrier height. Then we fitted the relationship between $\ln(Js/T^2)$ and $1/kT$ to a straight line and, estimated the barrier height to be 0.85 and 0.55 eV for Si/diamond interfaces annealed at 703 and 873 K, respectively. Additionally, we estimated A^* to be 9×10^{-7}, 4.1×10^{-6} $\mathrm{mAcm^{-2}K^{-2}}$ for Si/diamond interfaces annealed at 703 and 873 K, respectively. These values are more than 10 orders of magnitude smaller than the theoretical value (90000 $\mathrm{mAcm^{-2}K^{-2}}$). It was previously reported that the measured Richardson constant for diamond Schottky diodes was more than 3-10 orders of magnitude smaller than the theoretical value [26–28]. Such a large separation between the measurements and theory was explained by the scheme that a smaller fraction of the area of Schottky contacts was active at lower bias voltages based on characterization using a conductive AFM [26]. The small A^* obtained in the present work might be explained using a similar scheme since the separation between the measurements and theory is in the same order as that for diamond Schottky diodes.

Figure 5 shows the reverse *I-V* characteristics of diodes annealed at 873 K. As expected, the reverse current increased with increasing reverse-biased voltage and the current density reached to 60 $\mathrm{mA/cm^2}$ at 200 V. The breakdown characteristics were not observed.

4. Discussion

We previously reported that the Ar FAB irradiation of surfaces led to the formation of an amorphous-like layers at the bonding interfaces of diamond-based heterojunctions [29–31]. The thickness of the amorphous like layer decreased by annealing the junctions [29,30]. We also reported that the post-bonding annealing played a role of lowering potential barrier height and improving the conductive properties in isotype Si/Si, GaAs/GaAs, and Si/SiC junctions fabricated using SAB [24, 32, 33–]. Such a change in electrical properties of these junctions was attributed to the decrease of the density of interface states that were likely to be formed during the surface activation process. The observed improvement of the ideality factor, the reverse-bias current and barrier height by annealing, consequently, suggests that the effects of the interface states became small by annealing p^+-Si/p-diamond heterojunction diodes. Occurrence of two different barrier heights in the diodes annealed at 873 K [Fig. 3(a)] may be attributable to the possible inhomogeneity of the interface state charges. Contributions of the mechanical stress at interfaces and the thickness or composition of intermediate layers formed during the post bonding annealing [19], all of which could be inhomogeneous, should be investigated.

The observed rectification factor of Si/diamond heterojunction diodes after annealing at 873 K for 30 min are more than two orders of magnitude better than that of Cu/diamond Schottky diodes annealed at 923 K (Table I) [13]. Cu/diamond Schottky diodes have thermal stability approximately

equivalent to that of Si:W/diamond Schottky diodes [12]. The stability of parameters observed for Si/diamond diodes is in good contrast with previous reports of Al/diamond Schottky diodes, which showed degradation of reverse leakage currents after annealing at 723 K [14].

The reverse electric field at the Si/diamond interface E is expressed as

$$E=\sqrt{\frac{2qN_{\mathrm{A}}}{\varepsilon_{\mathrm{dia}}\varepsilon_0}\left(V+V_{\mathrm{bi}}-\frac{k_{\mathrm{B}}T}{q}\right)}. \quad (2)$$

In this expression, ε_0 and $\varepsilon_{\mathrm{dia}}$ are the permittivity of vacuum and the dielectric constant of diamond, N_{A} is the acceptor concentration, V_{bi} is the built-in potential and V is the applied voltage. We use $\varepsilon_{\mathrm{dia}}$ of 5.7 in literature [34]. We assume that N_{A} is 4×10^{16} cm^{-3}, or the nominal concentration of doped B atoms, and V_{bi} is 0.39 V based on the analysis of J_{S}-T relationship of 873 K annealed diodes. Using Eq. 2, E is estimated to be 2.3 MV/cm at V=200 V, the highest bias voltage in the reverse I-V characteristics shown in Fig. 5. It was reported that the breakdown characteristics occurred at 1.9 MV/cm for the Mo/p-diamond Schottky diodes using epitaxial substrates fabricated in same condition with this work [8]. The obtained results indicate that p$^+$-Si/p-diamond heterojunction diodes have excellent electrical stability.

We applied the thermionic field emission model with barrier-lowering effects considered (TFE+BL model) for analyzing the reverse-bias characteristics of heterojunction diodes as was done for diamond Schottky diodes [28,35,36]. The reverse leakage current in this model is expressed as

1 $$J_{\mathrm{TFE+BL}}=\frac{A^{*}Tq\hbar E}{k_{\mathrm{B}}}\sqrt{\frac{\pi}{2m^{*}k_{B}T}}\exp\left[-\frac{q}{k_{\mathrm{B}}T}\left(V_{\mathrm{bn}}-\left(\frac{qE}{4\pi\varepsilon_{\mathrm{dia}}\varepsilon_{0}}\right)^{\frac{1}{2}}-\frac{q(\hbar E)^{2}}{24m^{*}(k_{\mathrm{B}}T)^{2}}\right)\right]. \quad (3)$$

2 Here, $\hbar$ and m^{*} are the Dirac's constant and the effective mass of the carrier. We assume that m^{*} is

3 0.908 m_0 [37] where m_0 is the electron rest mass. The barrier height is estimated to be 0.66 eV by

4 using the the least squares method. $J_{\mathrm{TFE+BL}}$ curve calculated using the above equation for qV_{bn} of

5 0.66 eV are shown by dashed lines in Fig. 5.

6 We assume that no offset is formed in the vacuum level across p^{+}-Si/p-diamond bonding interface.

7 On this assumption, the barrier height for p^{+}-Si/p-diamond heterojunction diodes qV_{B} is expressed as

8 $$qV_{\mathrm{B}}=E_{\mathrm{g,dia}}-E_{\mathrm{g,Si}}-q\chi_{\mathrm{Si}}+q\chi_{\mathrm{dia}}+\delta_{\mathrm{p,Si}}\approx E_{\mathrm{g,dia}}-E_{\mathrm{g,Si}}-q\chi_{\mathrm{Si}}+q\chi_{\mathrm{dia}}. \quad (4)$$

9 In this expression, $E_{\mathrm{g,Si}}$ ($E_{\mathrm{g,dia}}$) is the bandgap of Si(diamond), $q\chi_{\mathrm{Si}}$($q\chi_{\mathrm{dia}}$) is the electron affinity

10 of Si(diamond) and $\delta_{\mathrm{p,Si}}$($\approx$0 eV) is the difference between the Fermi level and the valence band

11 maximum in p^{+}-Si, respectively. Given that reported $q\chi_{\mathrm{dia}}$ values are largely scattered [38–41], we

12 assume that $q\chi_{\mathrm{dia}}$=0 eV [38]. Using $E_{\mathrm{g,dia}}$=5.5 eV, $E_{\mathrm{g,Si}}$=1.12 eV, and $q\chi_{\mathrm{Si}}$=4.05 eV in literature [3],

13 we find that qV_{B}=0.36 eV, which is close to the barrier height for 873 K annealed diodes estimated

14 by analyzing the relationship between J_{S} and T using TE model (0.55 eV) and the reverse-bias

15 characeristics using TFE+BL model (0.66 eV). The obtained energy-band diagram of p^{+}-Si/p-

16 diamond interface at zero-bias voltage and at 300 K is shown in Fig. 6.

17

18 **5. Conclusion**

In summary, we successfully fabricated p^+-Si/p-diamond heterojunction diodes using the SAB and demonstrated their diode characteristics. We found that the ideality factor was improved, the reverse-bias current was decreased, and the barrier height at Si/diamond bonding interfaces was lowered by means of the post-bonding annealing, which suggested that the effects of interface states that were formed during the surface activation process were decreased. The rectification factor observed after annealing at 873 K was more than two orders of magnitude better than that of Cu/diamond Schottky diodes annealed at similar temperatures, which showed a high thermal stability of Si/diamond heterojunction diodes. The reverse *I-V* characteristics of p^+-Si/p-diamond heterojunction diodes annealed at 873 K agreed with a theoretical calculation based on the TFE model with the barrier lowering effects considered. The barrier height at Si/diamond bonding interfaces annealed at 873 K was estimated to be 0.55 and 0.66 eV by analyzing the relationship between J_S and T and the reverse-bias characteristics at room temperature, respectively. These values were close to that obtained by assuming that no offset was formed in the vacuum level across the Si/diamond bonding interfaces (0.36 eV). These results imply that heterojunction diodes using direct wafer bonding play a crucial role for promoting the development of diamond devices.

Acknowledgements

This work was supported in part by JSPS KAKENHI Grant No. 20K04581.

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2 **Table I.** The reverse-bias current, turn-on voltage, ideality factor, and resistance of p^+-Si/p-diamond

3 heterojunction diodes and Cu/diamond Schottky diodes [13].

	Annealing temperature	Ideality factor	Reverse-bias Current (mA/cm^2)	Turn-on voltage (V)	Rectifying factor
p^+-Si/p-diamond heterojunction diodes	Without annealing	2.62	1.12	1.75	10^4
	703 K	1.85	2×10^{-3}-3×10^{-3}	1.65	10^7
	873 K	1.25	2×10^{-3}-3×10^{-3}	1.15	10^7
	1073 K	1.3	7.57	0.46	10^3
Cu/p-diamond Schottky diodes [13]	923 K	1.3	5×10^{-3}-3×10^{-2}	1.2-1.3	10^5
	973 K	1.3	5×10^{-3}-3×10^{-2}	0.9-1.0	10^5
	1023 K	2.1	3	0.7-0.8	10^3

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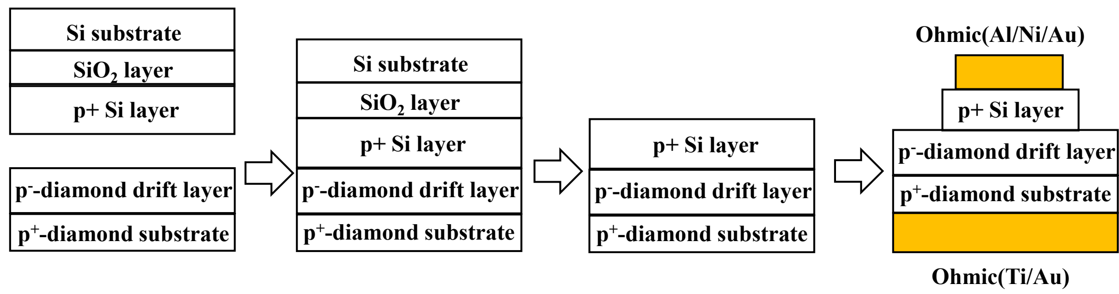

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2 **Figure 1.** The schematic flow of the process for fabricating diamond/Si heterojunction diodes.

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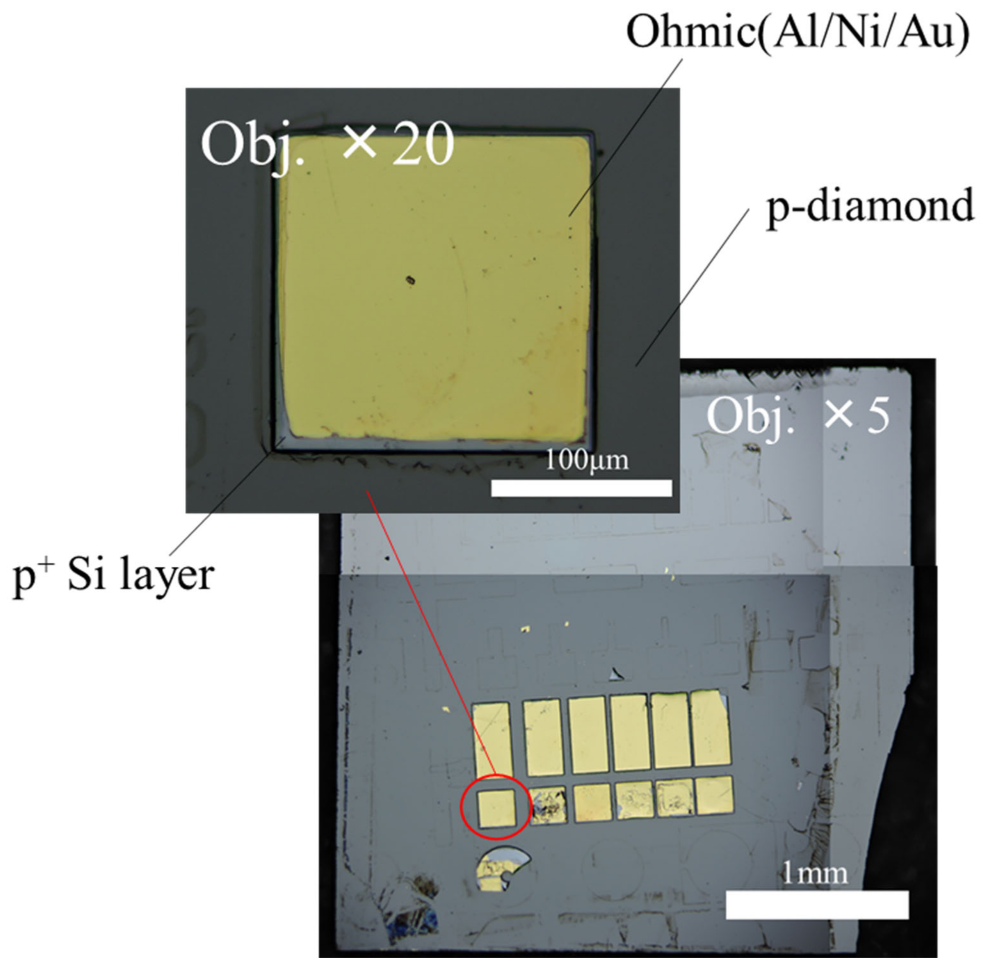

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2 **Figure 2.** An optical microscope image of diamond /Si heterojunction diodes.

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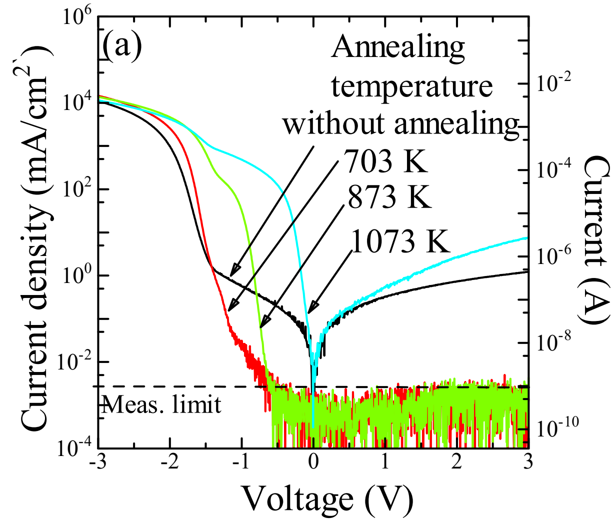

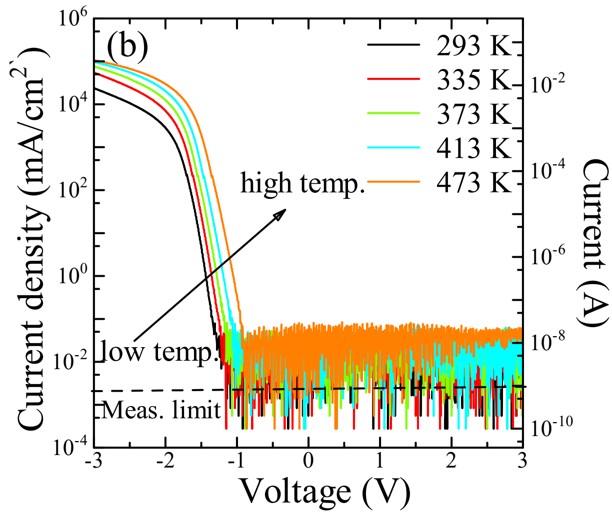

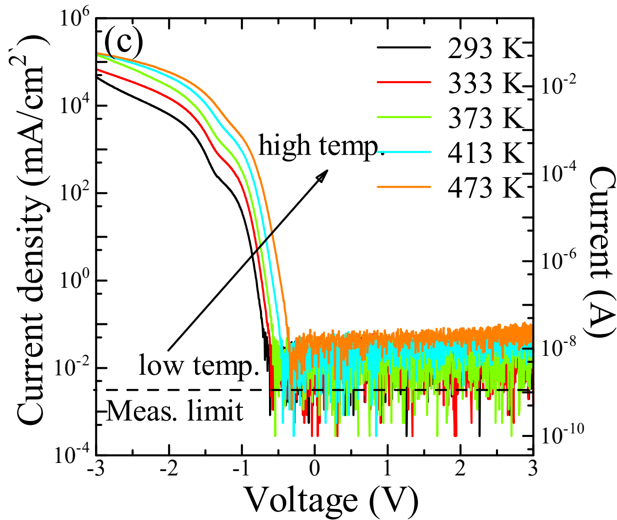

1 **Figure 3.** (a) Room-temperature *I-V* characteristics of p$^+$-Si/p-diamond heterojunction diodes without

2 being annealed, and annealed at 703, 873, and 1073 K. (b) and (c) The temperature-dependent *I-V*

1 characteristics of p^+-Si/p-diamond heterojunction diodes annealed at (b) 703 and (c) 873 K.

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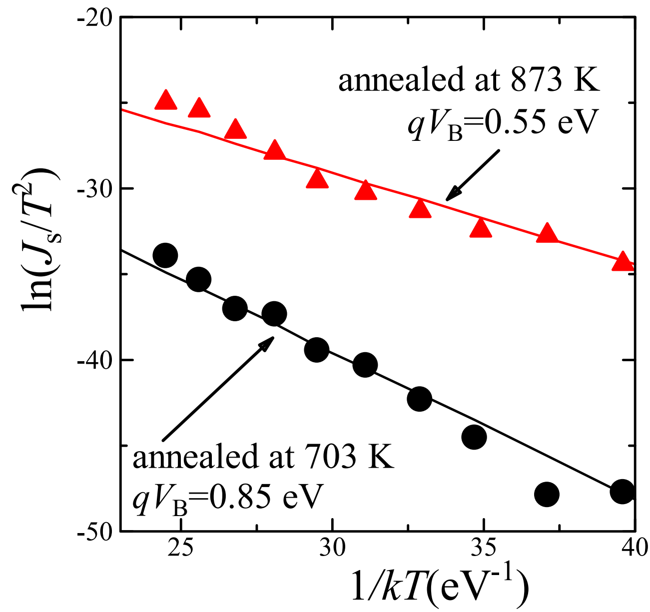

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7 **Figure 4.** Relationships between ln(Js /T^2) and 1/kT.

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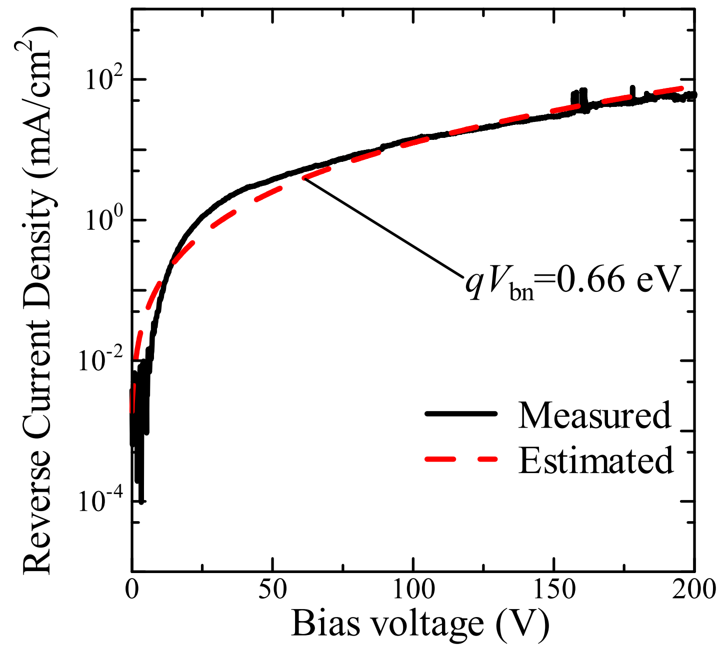

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2 **Figure 5.** The reverse *I*-*V* characteristics of p$^+$-Si/p-diamond heterojunction diodes annealed at 873

3 K.

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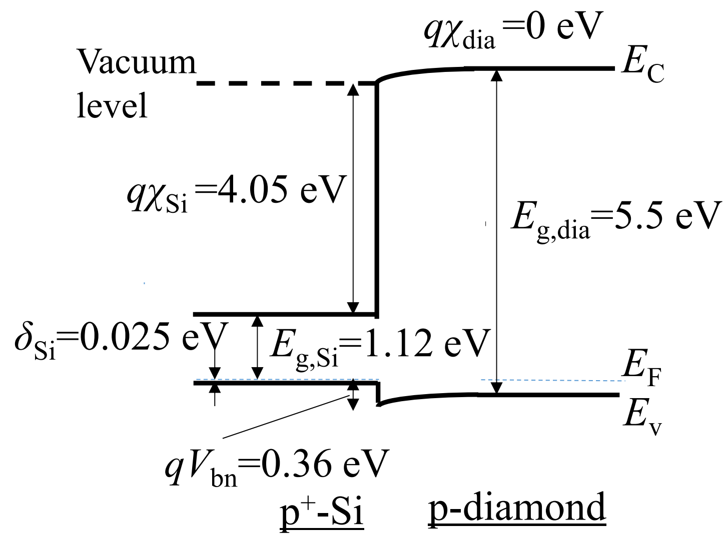

1 **Figure 6.** Schematic energy-band diagram of p^+-Si/p-diamond heterojunction diodes.

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