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Electrical Properties of p-Si/n-GaAs Heterojunctions by Using Surface-Activated Bonding

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The electrical properties of p-Si/n-GaAs heterojunctions fabricated by using surface-activated bonding (SAB) were investigated by measuring their current–voltage (*I–V*) and capacitance–voltage (*C–V*) characteristics. The *I–V* characteristics showed rectifying properties. Their flat-band voltage obtained from *C–V* measurements was around 1.6 V. Observation by using field-emission-scanning electron microscopy and energy dispersive X-ray spectroscopy revealed neither structural deficits nor oxide layers at the interfaces. These results suggest that the SAB-based Si/GaAs heterojunctions are applicable for fabricating novel devices. © 2013 The Japan Society of Applied Physics

The direct wafer bonding method has been employed for forming a variety of semiconductor junctions such as Si/Si,[1)] Si/SiO_2,[2,3)] GaAs/Si,[4)] InP/Si,[5)] GaAs/GaAs,[6)] and GaAs/InP[7,8)] junctions. These junctions, some of which are difficult to be made by conventional semiconductor growth technologies, such as molecular beam epitaxy and metal organic vapor phase epitaxy, were used for fabricating functional devices such as silicon-on-insulator structures,[2,3)] light-emitting diodes integrated on Si substrates,[5)] laser diodes,[7)] and tandem solar cells.[8)]

The process for removing native oxide layers on the bonding surfaces is essential prior to forming the above-cited junctions. Furthermore, processes at higher temperatures (typically $>500\,^{\circ}C$) during and/or after bonding are required for realizing junctions with better electrical characteristics.[6,8)] Such high-temperature processes, however, might cause the diffusion of impurities through the interfaces or mechanical deficits due to the difference in the thermal expansion coefficients of bonded substrates, which are assumed to limit the area of applications of the direct wafer bonding.

Surface-activated bonding (SAB),[9–13)] in which surfaces of substrates are activated by the fast atom beams of Ar prior to bonding, has enabled us to bond substrates without heating.[9)] Given that SAB has mainly been employed for fabricating micro-electro-mechanical systems, the prime concern in relevant research has been the mechanical and structural properties of junctions,[11,12)] although current–voltage (*I–V*) characteristics of SAB-based Si/Si, Si/GaN, and Si/InP junctions were reported.[10,13)]

In this work, p-Si/n-GaAs heterojunctions were fabricated by SAB, their electrical properties were characterized by *I–V* and capacitance–voltage (*C–V*) measurements. Furthermore their interface was investigated by field emission-scanning electron microscopy (FE-SEM) and energy dispersive X-ray spectroscopy (EDS). The applicability of the heterojunctions for novel functional devices such as Si/III–V tandem solar cells was explored based on these measurements.

We employed B-doped (100) p-Si and Si-doped (100) n-GaAs substrates. The Hall measurements at room temperature revealed that the resistivity and carrier concentration were 0.1 Ω·cm and ($N_{A,Si}$ =) $2.4 \times 10^{17}\,cm^{-3}$, and 0.002 Ω·cm and ($N_{D,GaAs}$ =) $1.1 \times 10^{18}\,cm^{-3}$, for the p-Si and n-GaAs substrates, respectively. These substrates were cleaned with acetone and ethanol in an ultrasonic bath for 300 s, dried under N_2, and then set in the introduction chamber of SAB facilities. It is noteworthy that prior to bonding, no procedure for removing native oxide layers on the surfaces of Si and GaAs substrates was utilized. The top surfaces of the substrates were activated by using an argon fast atom beam. After the surface activation, two substrates were brought into contact by pressing for 60 s. The temperature of the substrates was not intentionally raised while they were pressed. The in-plane directions of the substrates were not precisely aligned with each other. After the two substrates were bonded to each other, Al/Ni/Au and AuGe/Ni/Ti/Au multilayers were evaporated on the bottom surfaces of p-Si and n-GaAs substrates, respectively. The ohmic contacts were formed by a rapid thermal annealing at 400 °C for 60 s. Samples were then diced into 4 mm^2 pieces. Their *I–V* characteristics were measured by using an ADCMT 6242 Source Measurement Unit at temperatures between 298 and 473 K. The *C–V* characteristics were measured by using an Agilent E4980A Precision Impedance Analyzer at room temperature. An FE-SEM equipped with EDS facilities (JEOL JSM6500F) was employed for the cross-sectional characterizations for sides formed by dicing.

Figure 1(a) shows the cross-sectional FE-SEM image. The EDS results for the side of the GaAs substrate, the Si/GaAs interface, and the side of the Si substrate are shown in Figs. 1(b)–1(d), respectively. The areas for the respective EDS observations are marked as a1, a2, and a3 in Fig. 1(a). Areas a1 and a3 are separated from the Si/GaAs interface by approximately 2 μm. The atomic ratio of oxygen extracted for area a2 (4.59%) is close to that for a1 (4.19%), but larger than that for a3 (2.20%). More importantly, no structural deficits such as cracks were observed at the interface as shown in Fig. 1(a).

The *I–V* characteristic of one die at room temperature is shown in Fig. 2(a). The curve revealed rectifying properties similarly to those in conventional pn junctions. The onset for forward bias voltage was found to be 0.38 V. The inset shows the *I–V* characteristics measured at temperatures between 298 and 473 K. The respective curves revealed a more marked asymmetric nature at lower temperatures. It is noteworthy, however, that the magnitude of the current increased as the junctions were more deeply reverse biased. Furthermore, as the temperature was raised, the magnitude of the current for the reverse bias voltages increased while their slope remained almost invariant to temperature. The $1/C^2$–*V* characteristics measured at room temperature and at a frequency of 100 kHz are shown in Fig. 2(b). The characteristics revealed a straight line and the flat band

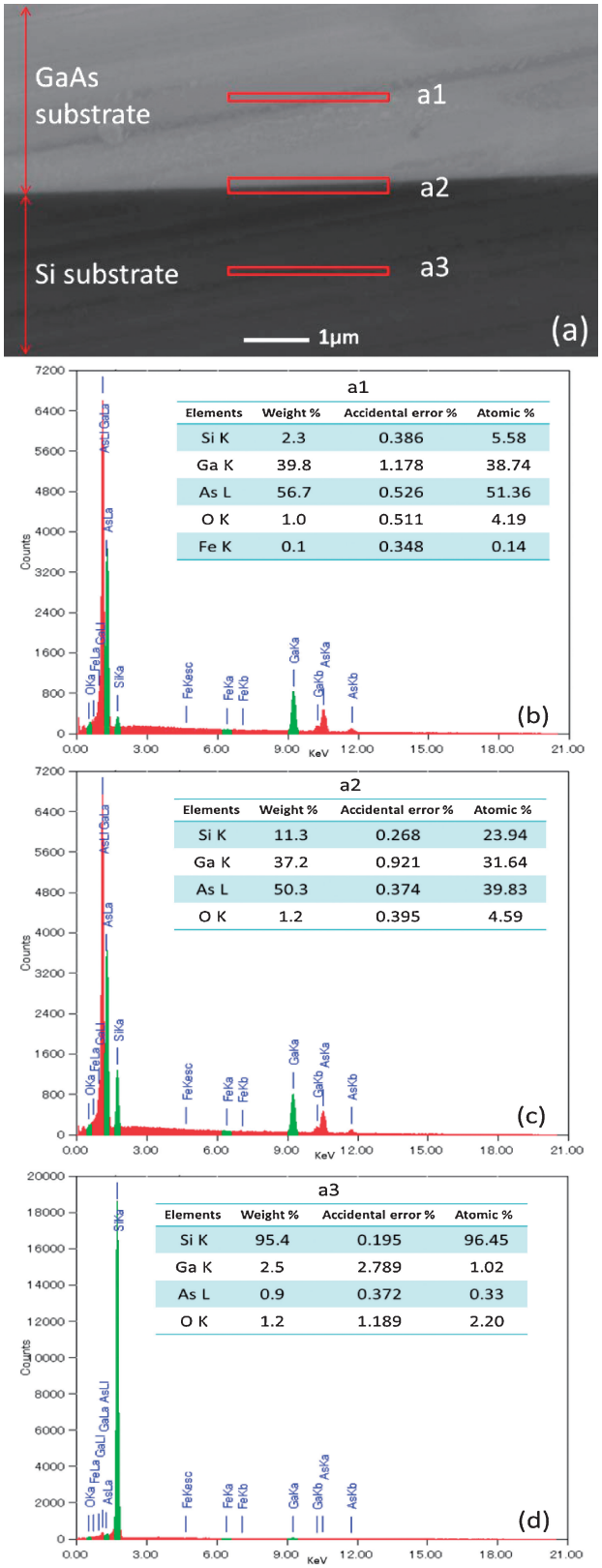

Fig. 1. FE-SEM cross-sectional image of the interface of Si/GaAs (a), and EDS composition maps in the GaAs around 2 μm apart from the interface of Si/GaAs (b), on the interface of Si/GaAs (c), and in the Si around 2 μm apart from the interface of Si/GaAs (d).

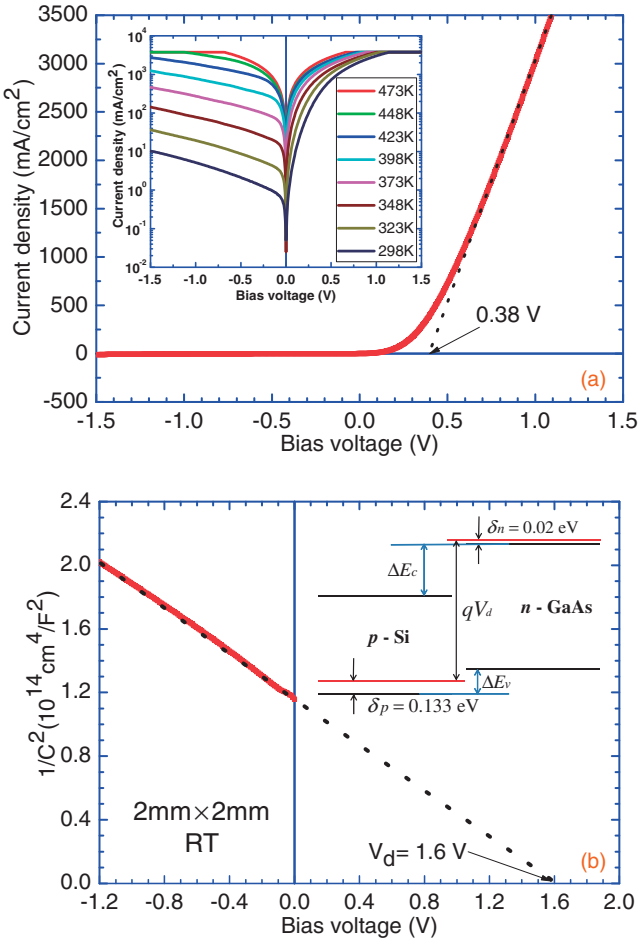

Fig. 2. (a) *I–V* characteristic of SAB-based p-Si/n-GaAs junctions measured at room temperature. The inset shows *I–V* characteristic of p-Si/n-GaAs junctions measured at temperatures between 298 and 473 K. (b) *C–V* characteristics of SAB-based p-Si/n-GaAs junctions measured at 298 K. The inset shows the difference in work functions between p-Si and n-GaAs.

voltage was found to be ~1.6 V by linearly extrapolating $1/C^2$ to zero.

The result that $1/C^2$ linearly depends on the bias voltage suggests that the crudest model is applicable for the diffusion potential in p-Si/n-GaAs heterojunction V_d, which is given by the difference in the work functions between p-Si and n-GaAs[14] and is expressed as

$$qV_d = E_{gp} + \Delta E_c + \delta_n - \delta_p, \quad (1)$$

where q is the elementary charge, E_{gp} is the energy gap of p-Si, ΔE_c is the conduction-band discontinuity, and δ_p and δ_n refer to the position of the Fermi energies relative to the valence-band maximum in p-Si and that relative to the conduction-band minimum in n-GaAs, respectively. [See the inset of Fig. 2(b).] Note that the above expression is based on the assumption that no electric charges are placed at the interfaces. Using Eq. (1), ΔE_c is estimated to be 0.593 eV, which is in semi quantitative agreement with that obtained for wafer-bonded GaAs/Si isotype heterojunctions (0.579 eV).[4]

In this framework, $d(1/C^2)/dV$ is given by

$$d(1/C^2)/dV = -\frac{2(\varepsilon_{GaAs}N_{D,GaAs} + \varepsilon_{Si}N_{A,Si})}{qN_{D,GaAs}N_{A,Si}\varepsilon_{GaAs}\varepsilon_{Si}}, \quad (2)$$

by referring to dielectric constants of Si (ε_{si}) and GaAs (ε_{GaAs}). By using Eq. (2), $d(1/C^2)/dV$ is found to be 6×10^{13} cm^4/(F^2·V) and is close to measurements [$\approx 6.7 \times 10^{13}$

$cm^4/(F^2 \cdot V)$]. In addition, the thicknesses of the depletion layers are estimated to be ≈84 and ≈18 nm in p-Si and n-GaAs layers (not depicted), respectively, in the case of zero-bias voltages. The resultant capacitance amounts to $\approx 1.1 \times 10^{-7}$ F/cm^2, which is close to the measurements.

Here, we note that the characteristic X-ray signals in EDS measurements are generated in a region with a depth of a few micrometers, and that the signals due to oxygen in the a1 and a3 EDS results are likely to be attributed to the native oxide layer with atomic-layer thicknesses formed on the surface of GaAs and Si, respectively. We are then led to the hypothesis that stronger signals due to oxygen should be observed in the a2 EDS results [Fig. 1(c)] if the oxide layer were to be formed on the Si/GaAs interface. The result that the atomic ratio of oxygen in the a2 area is close to that in the a1 area, consequently, suggests that the Si/GaAs interface is free from the hypothetical oxide layer, which is supported by the results of the transmission electron microscopy-EDS observation for SAB-based Si/Si junctions.[13] The difference in the atomic ratio of oxygen between a1 and a3 areas might be attributable to the amount of oxygen in native oxides of Si and GaAs.[15]

The features in the *I*–*V* characteristics such as (1) increase in current due to deeper reverse bias and (2) slope in current almost invariant to temperature are similar to those for SAB-based p-Si/n-Si junction.[13] We found that those features were consistent with the scheme of trap-assisted tunneling[16] with a trap energy of ∼0.1 eV in comparison with analyses by using other schemes for the carrier transport in reverse-biased junctions such as generation-recombination model,[17] Frenkel–Poole model,[18] and band-to-band tunneling model.[19] Such kind of tunneling process is likely to explain the low onset observed in *I*–*V* characteristics with forward bias voltages. The difference between the onset *I*–*V* characteristics and the flat-band voltage in *C*–*V* characteristics suggests that the response of traps at the interface is slower than the frequency for *C*–*V* measurements.

Although there are leak currents in the SAB-based p-Si/n-GaAs heterojunctions, which is attributable to tunneling through ∼0.1 eV traps, it is notable that (1) the junctions revealed rectifying properties, and (2) their inverse of square of capacitance almost linearly depended on the bias voltage. Such features in electrical properties are likely to be consistent with the results of FE-SEM EDS analysis showing no evidence of possible oxide layers at the Si/GaAs interfaces. These findings, together with the result of SEM observation showing that the two substrates were firmly bonded to each other, suggest that the SAB-based Si/GaAs heterojunctions are applicable for fabricating novel functional devices.

In summary, p-Si/n-GaAs heterojunctions were successfully fabricated by using the SAB without heating the substrates. Their current–voltage characteristics showed rectifying properties. Their capacitance–voltage characteristics were consistent with a simple model for the diffusion potential, which is based on the assumption that no electrical charges are located at the interfaces. These findings, together with the results of the cross-sectional observation by using FE-SEM EDS, suggest the potentiality of the SAB method.

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