Effects of post bonding annealing on GaAs//Si bonding interfaces and its application for sacrificial-layer-etching based multijunction solar cells

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ABSTRACT

By using the sacrificial layer (SL) etching, GaAs substrates are separated from III-V epi substrate//Si substrate junctions that are made by surface activated bonding (SAB) technologies. The post-bonding low-temperature (300-°C) annealing plays an essential role in achieving a promising (∼90%) bonding yield. The effects of the post-bonding annealing are investigated by hard X-ray photoemission spectroscopy and current-voltage measurements of GaAs//Si bonding interfaces. It is found that the concentration of oxygen atoms at interfaces is reduced and the resistance decreases to 1.6-2.1 mΩcm^2 by the low-temperature annealing. Aluminum fluoride complexes are not observed by X-ray photoelectron spectroscopy on the exposed surfaces of separated GaAs substrates. The roughness average of the surfaces is ≈0.25-0.30 nm. The characteristics of double junction cells fabricated on the GaAs//Si junctions prepared by the SL etching are almost the same as those of cells fabricated by dissolving GaAs substrates after bonding. These results indicate that multijunction cells could be fabricated in a process sequence compatible with reuse of GaAs substrates by combining the SL etching and SAB.

1. Introduction

Multijunction (MJ) cells composed by stacking subcells with different bandgaps [1–19] are the most promising for realizing photovoltaics with high conversion efficiencies [20]. In most cases, subcells at the upper part with wider bandgaps are made of group-III arsenide or phosphide (III-V) compound semiconductors (CSs). Narrower-bandgap III-V or group IV semiconductors such as Ge and Si are used for the lower-part or bottom subcells. MJ cells with various combinations of subcells such as InGaP/(In)GaAs/Ge [2], InGaP/GaAs/InGaAs [4], InGaP/(Al)GaAs/Si [7, 11, 12, 14, 16, 17, 19], and In(Al)GaP/GaAs/InGaAsP/InGaAs [8, 13], were fabricated and excellent characteristics were demonstrated.

In a previous research of MJ cells, the entire subcell stacks were fabricated using the epitaxial growth [1, 2, 4, 5]. We have to note, however, that the epitaxial growth is in general quite difficult because of the difference in crystal symmetries, lattice constants and/or thermal expansion coefficients among subcells [21]. Instead of the epitaxial growth, several types of wafer bonding technologies such as conventional direct bonding in the atmosphere [3, 6] and smart stack approach using Pd nanoparticles [16, 17, 19] have been used. The surface-activated bonding (SAB) [22], in which the substrates are directly bonded in vacuum just after activating their surfaces, have widely been used for bonding subcell layers [7–10, 12–14, 18].

We previously reported that interfacial layers formed at bonding interfaces caused a parasitic series resistance [23]. The resistance was, however, lowered below acceptable levels by heating junctions during or after bonding at 400 °C or higher temperatures [3, 23, 24]. It was reported that the characteristics of GaAs cells bonded to Si substrates almost agreed with those of as-grown GaAs cells [25], which suggested that possible influence due to the wafer bonding was negligibly small.

In a conventional and simple version of the aforementioned wafer-bonding based, or hybrid, approaches, CS substrates hosting the growth of the upper subcells, typically GaAs substrates, are dissolved after bonding the upper subcells to the lower subcells [10, 12]. It is notable that the fabrication cost of MJ cells could be drastically reduced if the reuse of CS substrates is possible [15].

The epitaxial lift-off (ELO) technologies have been applied for the reuse of CS substrates [26–32]. In a typical ELO process for solar cells, thick supporting layers such as back metals are first formed on surfaces of III-V cell layers. Then the cell layers are stripped from the GaAs substrates by selectively etching the sacrificial layers (SLs) sandwiched between cell layers

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and substrates. The separated GaAs substrates are reused for another epitaxial growth. Stripped cell layers are mounted on metal plates [26], plastic films [31], or other temporal substrates [32] via metal layers so that thin film solar cells are fabricated. Low-cost hybrid MJs might be realized by growing subcell layers on thin GaAs films transferred to Si [33]. High-density cracks, however, were apparent on surfaces of GaAs cell structures grown in this scheme [34], which were likely to limit cell yield. It is assumed, consequently, that a practical solution is given by growing subcell structures on GaAs substrates, directly bonding them to Si bottom cells, then separating the GaAs substrates by etching SLs.

In typical ELO processes, AlAs and hydrofluoric (HF) solution are used as SL and its etchant, respectively. In the etching process of AlAs, it was reported that an aluminum fluoride complex with low solubility $AlF_3 \cdot 3H_2O$ is formed by the following chemical reaction:

$$AlAs+3HF+6H_2O \rightarrow AsH_3+AlF_3 \cdot (H_2O)^3+3H_2O, \tag{1}$$

and prohibits the progress of etching as residues deposited on the etch front [28, 29]. A weight induced ELO (WIELO), in which a force is applied normal to SL, has been developed so as to minimize effects of the residues and quickly strip the epi layers [35, 36]. In case of III-V//Si junctions, the bonding interfaces are assumed to be placed in the HF-based etchant for longer ($\sim 10^{1-2}$ hours) periods in comparison with the WIELO process. This means that a higher tolerance against HF etchant is required for the bonding interfaces.

In this work, we investigate the validity of the combination of SAB and subsequent SL etching in fabricating III-V//Si hybrid junctions and MJ cells. Effects of low-temperature ($\leq$300 °C) post-bonding annealing on the bonding yield and the properties of bonding interfaces are highlighted. The properties of exposed surfaces of separated GaAs substrates as well as performances of GaAs//Si 2J cells [37] are also discussed.

2. Methods

All of the bonding specimens employed in the work were prepared using conventional SAB technologies with a fast atom beam (FAB) of Ar. Substrates were not heated in the bonding process. The bonding parameters such as the background pressure, acceleration voltage of FAB, and load were the same as those previously applied for fabricating III-V//Si junctions [10, 12].

In a preparatory study, we prepared a 200-nm GaAs/20-nm AlAs heterostructure on a GaAs (100) substrate by metal organic vapor phase epitaxy. The GaAs/AlAs heterostructure was diced into 1 cm by 1.2 cm dies and bonded to Si (100) substrates. After annealing at 300 °C, the junctions were placed in a 7.7% HF solution. The duration required for separating GaAs substrates was typically $\sim$30 hours. Following the concept of WIELO, we applied a force (2N) to the 1-cm wide edge of the GaAs substrate of junctions during this period. Note that the direction of the force was parallel to the bonding interface in this case. The exposed surfaces of separated GaAs substrate were routinely rinsed with an organic alkaline solution and characterized using atomic force microscope (AFM) and X-ray photoelectron spectroscopy (XPS).

We fabricated thin GaAs film//Si junctions by grinding and etching bonded GaAs substrates. Thickness of GaAs films d_{GaAs} was $\approx$15 nm. The junctions were annealed at 300 °C before grinding. Effects of the annealing on the chemical properties of GaAs//Si interfaces were examined by means of the angle-resolved hard X-ray photoemission spectrocopy (HAXPES) at BL47XU facilities in SPring-8 [38, 39]. The energy of incident X-ray photons was 7940 eV. We focused on Ga $2p_{3/2}$ core spectra. The measurement was performed for the take-off angle θ between 4 and 76° with a 6° step.

We also fabricated an n^+-GaAs//n^+-Si junction by bonding an n^+-GaAs epi layer grown on an n-GaAs (100) substrate to an n^+-Si (100) substrate. The donor concentration of the n^+-GaAs layer and the n^+-Si substrate were $\sim 10^{19}$ cm^{-3} and $\sim 10^{20}$ cm^{-3}, respectively. Before bonding, ohmic contacts had been formed on backsides of respective substrates by evaporating AuGe/Ni/Ti/Au (n-GaAs) and Ti/Au (n^+-Si) and annealing at 400 °C. After bonding, we annealed the junctions at different temperatures up to 300 °C. We measured their junction resistance and examined the effects of low temperature annealing on electrical properties of n^+-GaAs//n^+-Si bonding interfaces.

In fabricating solar cells, we first prepared an n-on-p GaAs 1J structure on a GaAs (100) substrate. The 1J structure was composed of AlAs SL, n-InGaP etch stopper layer, n^+-GaAs contact layer, n-doped phosphide window/emitter layer, p-GaAs base, p-doped back surface field layer, and p^+-GaAs/n^+-GaAs tunnel junction. Note that the 1J structure was grown in the inverse direction. The GaAs 1J epi substrate was bonded to an n-on-p Si 1J substrate, which had been prepared by implantation of P and B ions to a p^--Si (100) substrate and annealing for activation. Using the 300-°C annealing and subsequent SL etching, the GaAs substrate was separated. 2J cells were fabricated by forming contacts, performing the mesa etching, and selectively etching the n^+-GaAs contact layer. The emitter contacts were prepared by evaporating AuGe/Ni/Ti/Au on the n^+-GaAs contact layer. The base contacts were formed by evaporating Al/Ni/Au on the backside of p-Si substrates. It was notable that anti-reflection coating was not employed since our purpose was to examine

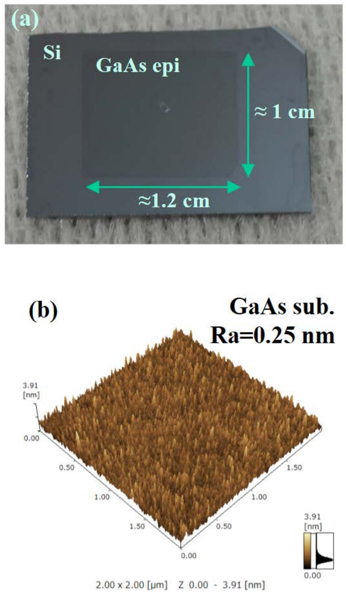

Figure 1: (a) A top view of GaAs epi//Si junction obtained by etching the SL after a post-bonding annealing at 300 °C for 1 hour. (b) An AFM image of the surface of GaAs substrate exposed by etching the AlAs SL in the GaAs//Si junction annealed for 1 hour.

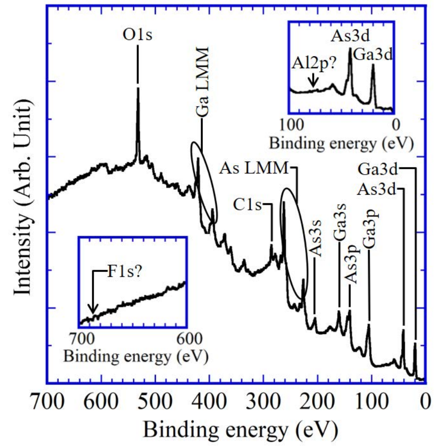

Figure 2: XPS spectra of the exposed surface of separated GaAs substrate. Spectra for binding energy between 0 and 100 eV and for binding energy between 600 and 700 eV are shown in insets.

the validity of SL etching in fabricating hybrid MJ cells in the simplest manners. We also made GaAs//Si 2J cells by grinding and dissolving the GaAs substrate after bonding the GaAs 1J epi substrate for comparison. We measured the current-voltage (I-V) characteristics under the air mass (AM) 1.5G/one sun solar irradiance and in the dark as well as the spectral response of the respective cells using in-house facilities. The error in measurements was ∼5%.

3. Results

3.1. Separation of GaAs substrate from III-V//Si junction

A top view of the GaAs epi layer bonded to Si made of the junction annealed for 1 hour is shown in Fig. 1(a). An ∼90% of the GaAs epi layer was successfully bonded to the Si substrate. In contrast, in case of the GaAs//Si junction annealed for 1 min., a ∼20-40% of GaAs epi layer remained bonded to Si after separating the GaAs substrate. No epi layer was left bonded to Si after the SL etching when the junction was not annealed (not shown). These results indicate that a post-bonding annealing for a long period (∼1 hour) is useful in separating GaAs substrates by etching the SLs.

An AFM image of the exposed surface of separated GaAs substrate is shown in Fig. 1(b). Its roughness average (Ra) was 0.25 nm. It is notable that the Ra of the surface of GaAs substrate is close to a typical Ra of epi-ready GaAs substrates (∼0.3-0.4 nm).

XPS spectra of the exposed surface of GaAs substrate are shown in Fig. 2. Spectra for binding energy between 0 and 100 eV and for binding energy between 600 and 700 eV are shown in insets. Peaks due to Ga, As, O, C are apparent. However no signals due to aluminum fluoride complexes, which could appear at ≈76.9-77.1 and ≈686.3-687.8 eV for Al (Al 2p) and F (F 1s) species, respectively [40], are observed. This finding means that a measurable amount of insoluble AlF_3 deposits was not adhered to the exposed surface.

3.2. Effects of post-bonding annealing on GaAs//Si interfaces

The angle-resolved Ga $2p_{3/2}$ core spectra of the GaAs//Si interface after annealing for 1 hour are shown in Figs. 3(a)-3(m). The spectra for the 1-min. annealed GaAs//Si interface are shown in Figs. 4(a)-4(m). By means of the least square fit to a Voigt (Gaussian-Lorentzian) function with Shirley background, we find that each spectrum is composed of two peaks with binding energies of ≈1116.9 and 1118.4 eV, which are due to the Ga-As and Ga-O bonds, respectively [41, 42]. Results of fitting are also shown for the respective spectra.

The relationship between the relative intensity of Ga-As signal, Ga-As/(Ga-As+Ga-O), and θ is shown in Fig. 5. Intersecting straight lines are eye guides of the angular dependence of Ga-As/(Ga-As+Ga-O). We find that for the 1-hour annealed interface, Ga-As/(Ga-As+Ga-O) increases as θ increases up to 28° (hereafter referred to as θ_0). It remains constant for $\theta > \theta_0$. For the 1-min. annealed interface, Ga-As/(Ga-As+Ga-O) increases as θ increases up to $\theta_0 = 35°$. It remains constant for $\theta > \theta_0$.

Ga-As/(Ga-As+Ga-O) is ≈0.4-0.5 and 0.2-0.4 for the 1-hour annealed interface and 1-min. annealed interface, respectively, i.e., the Ga-As signal is more apparent in the 1-hour annealed interface. We have to note that there is likely to occur a difference in d_{GaAs}

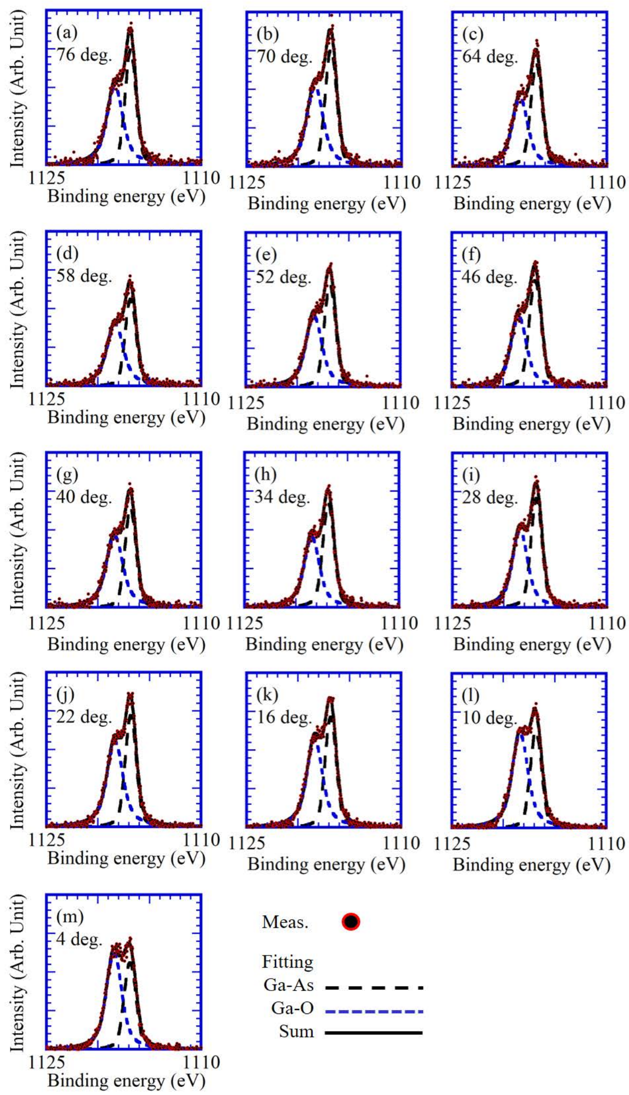

Figure 3: Angle-resolved Ga 2p$_{3/2}$ core spectra of ~15-nm GaAs//Si junctions annealed for 1 hour collected by HAXPES. θ is (a) 76°, (b) 70°, (c) 64°, (d) 58°, (e) 52°, (f) 46°, (g) 40°, (h) 34°, (i) 28°, (j) 22°, (k) 16°, (l) 10°, and (m) 4°.

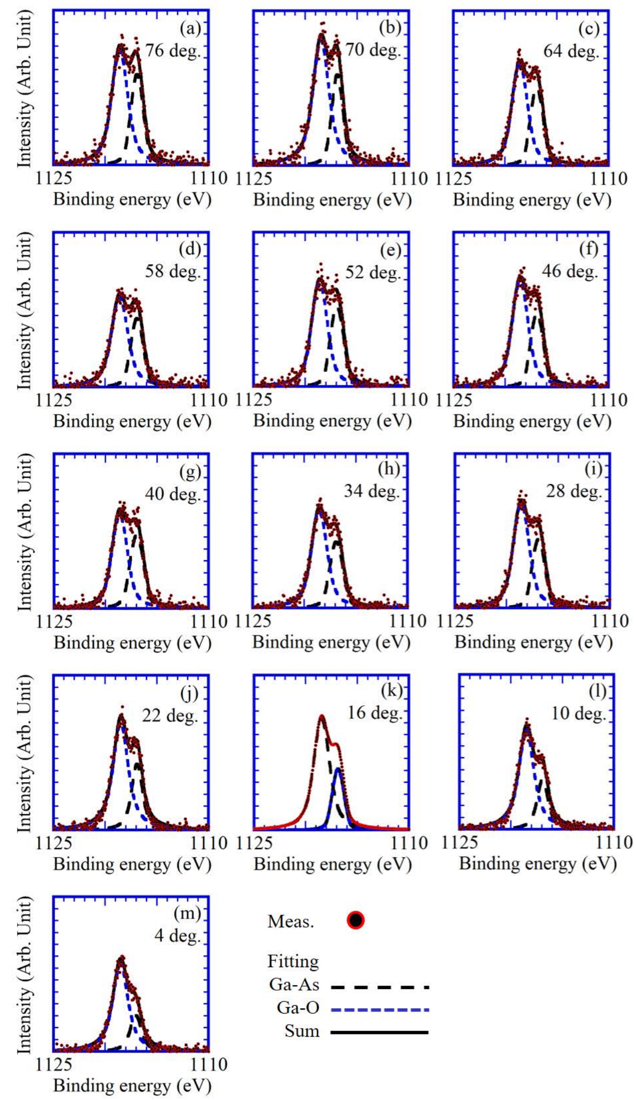

Figure 4: Angle-resolved Ga 2p$_{3/2}$ core spectra of ~15-nm GaAs//Si junctions annealed for 1 min. collected by HAXPES. θ is the same as those for Fig. 3.

between the two junctions and such a difference should also influence Ga-As/(Ga-As+Ga-O). An analysis on the angular dependence of Ga-As/(Ga-As+Ga-O), discussed in the appendix, suggests that d_{GaAs} of the 1-hour annealed junction is estimated to be 12.5 nm and smaller than d_{GaAs} of the 1-min. annealed junction (15.3 nm). A larger Ga-As/(Ga-As+Ga-O) is obtained for the 1-hour annealed junction and the contribution of annealing manifests itself more clearly by compensating the difference in d_{GaAs} of the two junctions.

We observed ohmic features in I-V characteristics of n$^+$-GaAs//n$^+$-Si junctions irrespective of the annealing condition. The junction resistance is summarized in Fig 6. We obtained lower resistances by annealing at higher temperatures and for longer periods. A resistance of as low as 1.6-2.1 mΩcm^2 was observed for junctions annealed at 300 °C for 1 hour. The obtained resistance is comparable to a resistance in GaAs//Si junction fabricated by SAB with substrate heating (3.6 mΩcm^2) [24] and a resistance in a GaAs//grid metal/Si junction (1-3 mΩcm^2) [43]. A higher resistance was observed after annealing for a longer period (3 hours), which might be due to the difference in thermal expansion coefficients between GaAs and Si. We also characterized junctions that were fabricated by SAB with substrate heating at 200 °C and were subsequently annealed. The lowest resistance was 0.9-1.6 mΩcm^2. (See Fig. S1 in the supplementary material).

3.3. GaAs//Si 2J cells

Figure 7(a) compares the I-V characteristics of SL-etching based GaAs//Si 2J cells with those of 2J cells fabricated by conventionally dissolving the GaAs substrate after bonding. Values of parameters characterizing performances of these cells are summarized in Ta-

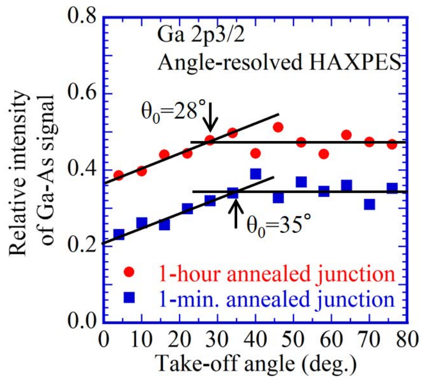

Figure 5: The dependencies of relative intensity of Ga-As signal, Ga-As/(Ga-As+Ga-O), in the Ga $2p_{3/2}$ core spectra on the take-off angle.

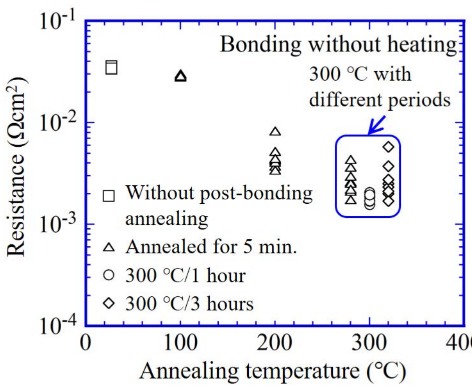

Figure 6: The dependence of resistance of n^+-GaAs//n^+-Si junctions on the annealing condition.

Table 1
Characteristics of GaAs//Si 2J cells.

	GaAs//Si 2J	
	SL etching	Dissolving GaAs sub.
Short-circuit current (mA/cm^2)	10.0	9.9
Photocurrent generated in subcells (mA/cm^2)		
GaAs subcell	16.4	15.7
Si subcell	3.6	3.8
Open-circuit voltage (V)	1.27	1.24
Efficiency (%)	10.7	10.1
Parasitic resistance (Ωcm^2)	0.73	0.80
Sum of ideality factors	3.1	3.7

ble 1. The short-circuit current and open-circuit voltage of the SL-etching based cells are 10.0 mA/cm^2 and 1.27 V. Those of the GaAs-substrate-dissolution based cells are 9.9 mA/cm^2 and 1.24 V.

The external quantum efficiency (EQE) spectra of these cells are compared in Fig. 7(b). The highest EQE is ≈55% since the cells are not coated with anti-

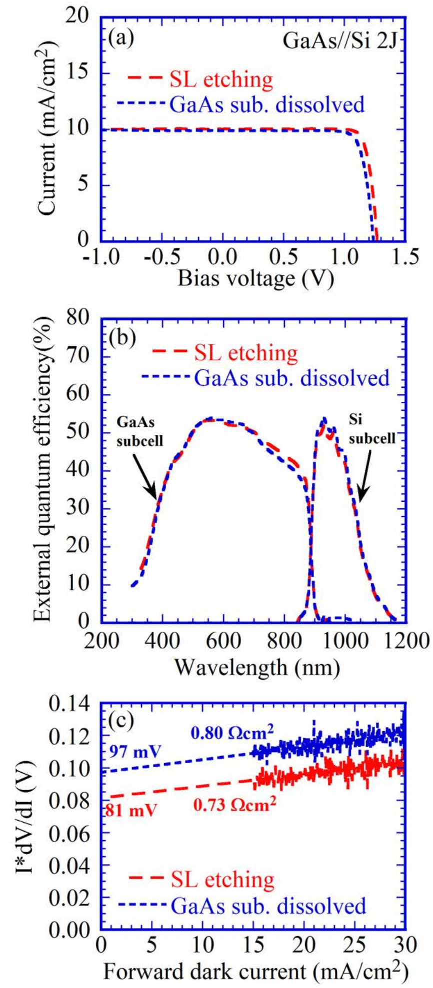

Figure 7: (a) I-V characteristics of GaAs//Si 2J cells fabricated by the SL etching and by dissolving the GaAs substrate. (b) EQE spectra of GaAs//Si 2J cells. (c) The relationship between IdV/dI and I extracted from the forward-bias characteristics of the respective cells in the dark.

reflection films. More importantly, we separately observe the contribution of each subcell in the EQE spectra of both of 2J cells, which indicates that these 2J cells work normally. The EQE of GaAs subcells are comparable to that of a GaAs 1J cell bonded to an n^+-Si substrate (See Fig. S2(b) of the supplementary material). Photocurrents to be generated under the AM 1.5G/one sun solar irradiance in the respective subcells, which were estimated by integrating their EQE spectra, are shown in Table 1. The mismatch in currents between GaAs and Si subcells is observed. Photocurrents in GaAs subcells (15.7-16.4 mA/cm^2) are close to a short-circuit current of the GaAs 1J cell (15.1 mA/cm^2 as is shown in Fig. S2(a)).

We extracted IdV/dI from the I-V characteristics for forward-bias voltages in the dark. The relationship between IdV/dI and I is shown in Fig. 7(c). Using the standard model for pn diodes, IdV/dI for forward-bias voltages is expressed as

$$I\frac{dV}{dI} = \frac{nkT}{q} + IR_p, \tag{2}$$

where n is the ideality factor. kT/q and R_p are the thermal voltage (26 mV at 300 K) and the parasitic series resistance, respectively [18]. In case of GaAs//Si 2J cells, we obtain

$$I\frac{dV}{dI} = \frac{(n_{\mathrm{GaAs}} + n_{\mathrm{Si}})kT}{q} + IR_p, \tag{3}$$

where $n_{\mathrm{GaAs}} + n_{\mathrm{Si}}$ is the sum of ideality factors of GaAs and Si subcells. Using this equation, the sum of ideality factors and the parasitic resistance of the respective 2J cells are obtained. The results are also shown in Table 1. The sum of ideality factors is 3.1 and 3.7 for the SL-etching based 2J cell and the GaAs-substrate-dissolution based 2J cell, respectively. The obtained values fulfill the requirement that $1 \leq n_{\mathrm{GaAs}}, n_{\mathrm{Si}} \leq 2$. The parasitic resistance is 0.73 and 0.80 $\Omega\mathrm{cm}^2$ for the SL-etching based 2J cell and the substrate-dissolution based 2J cell, respectively. These values of parasitic resistance of the 2J cells are $\times 300 \sim 400$ higher than the resistance of annealed n^+-GaAs//n^+-Si junctions (Fig. 6), which is attributable to finite thicknesses of heavily-doped bonding layers in 2J cells.

4. Discussion

Ga-O peaks in Ga $2\mathrm{p}_{3/2}$ core spectra in HAXPES are attributable to native oxides on the surface of GaAs layers and oxides on the GaAs//Si interfaces. Given that the contribution of the native oxides to HAXPES is likely to be insensitive to the period of 300-°C annealing, the higher Ga-As/(Ga-As+Ga-O) of the junction annealed for a longer period (1 hour) indicates that oxides at the GaAs//Si interfaces got diminished, which suggests that the oxides at interfaces were decomposed and the oxygen atoms were diffused into GaAs layers. This view is likely to be justified by a reported expression for the diffusion coefficient of oxygen in GaAs [44]. The reduction of concentration of oxygen atoms after annealing was also reported for GaAs//InP bonding interfaces [3].

Noting that oxides are selectively etched in a HF-based solution, this result also provides an atomic-scale basis for the high bonding yield in annealed III-V//Si junctions after the SL etching. The lower electrical resistance across the interfaces is also due to the reduction of oxides at bonding interfaces.

We note that AFM and XPS analyses showed that Ra of exposed surfaces of separated GaAs substrate was close to that of epi-ready substrates and no symptoms of possible deposits of AlF_3 complexes were observed on the surfaces. These findings suggest that separated GaAs substrate could be reused for the epitaxial growth. The result that the parasitic resistances of the two types of 2J cells were close to each other is also explained by the result of XPS analysis. The observed short-circuit currents and efficiencies of 2J cells, which are similar to each other, are comparable to those of GaAs/Si 2J cells fabricated using the smart stack [16]. The obtained results, consequently, indicate that the SL etching in combination with the SAB is potentially promising for fabricating III-V based hybrid MJ cells and reusing the separated GaAs substrate.

We find that the SL-etching based 2J cell slightly outperforms the substrate-dissolution based 2J cell in terms of the open-circuit voltage, the ideality factor, and the parasitic resistance (Table 1). A mechanical stress that could be introduced during grinding GaAs substrates might deteriorate the properties of bonding interfaces of substrate-dissolution based 2J cells.

5. Conclusion

We explored the possibility of combining the SL etching and SAB for fabricating hybrid MJ cells while GaAs substrates for growing the upper-part subcells are reused. By annealing junctions with GaAs//Si bonding interfaces at low temperature (300 °C) for a long period (1 hour), a promising part (∼90%) of the III-V epi layers remained bonded to Si substrates after separating the GaAs substrate. Effects of such low temperature annealing on the bonding interfaces were confirmed by performing HAXPES analyses of the bonding interfaces and measuring their electrical properties. The results of AFM and XPS observations of the exposed surfaces of separated GaAs substrates suggested that the separated GaAs substrates can be reused for epitaxial growth. We fabricated GaAs//Si 2J cells using the SL etching. Their characteristics almost agreed with those of cells fabricated by means of the conventional process sequence in which the GaAs substrates were dissolved after bonding.

Acknowledgements

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A. Adjustment of thicknesses of GaAs layers in GaAs//Si junctions for HAXPES analyses

We assume that the bonded GaAs film in samples for HAXPES analyses are composed of (i) a mixture of native oxide and GaAs on the surface, (ii) a pure GaAs layer, and (iii) a mixture of oxide and GaAs at the bonding interface. Noting that the HAXPES signals

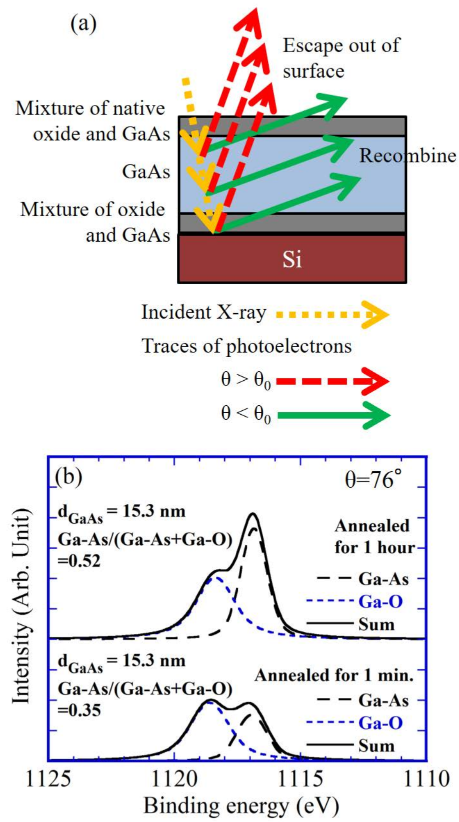

Figure A.1: (a) Schematic behaviors of photoelectrons in GaAs film//Si junctions for $\theta > \theta_0$ and for $\theta < \theta_0$. (b) A Ga $2p_{3/2}$ core spectrum at $\theta = 76°$ calculated for the 1-hour annealed GaAs//Si junction with d_{GaAs}=15.3 nm and a result of fitting to the spectrum for the 1-min. annealed junction.

for smaller θ correspond to the properties of shallower part of samples, the result that Ga-As/(Ga-As+Ga-O) increases as θ increases up to θ_0 (Fig. 5) suggests that for $\theta < \theta_0$ HAXPES signals for smaller take-off angles represent the surface and a shallower part the middle GaAs layer. Photoelectrons generated at the deeper part of GaAs layer and at the interface recombine inside the GaAs film and cannot escape out of the sample. In contrast, signals for $\theta > \theta_0$ should show the properties of the entire GaAs film since Ga-As/(Ga-As+Ga-O) for such take-off angles is constant. This view is schematically shown in Fig. A.1(a).

On this view we are led to the contention that d_{GaAs} should be proportional to $\sin\theta_0$. Assuming that $d_{\mathrm{GaAs}} = 3\lambda \sin\theta_0$, where λ is the inelastic mean free path of photoelectrons in GaAs (8.9 nm for electrons with a kinetic energy of 6820 eV corresponding to a binding energy of 1120 eV) [45, 46], d_{GaAs} is estimated to be ≈ 12.5 and ≈ 15.3 nm for the 1-hour and 1-min. annealed interfaces, respectively.

In a hypothetical case that d_{GaAs} of the two junctions is equally 15.3 nm, the HAXPES signal due to Ga-As bonds in the 1-hour annealed junction is assumed to be enhanced by a factor of $\sin(35°)/\sin(28°) = 1.22$ at $\theta > \theta_0$ while the signal due to Ga-O bonds is unchanged. The Ga$2p_{3/2}$ spectrum of the 1-hour annealed junction for $\theta = 76°$ was calculated for $d_{\mathrm{GaAs}} = 15.3$ nm. The obtained core spectrum is compared with a fit to the as-measured spectrum for the 1-min. annealed interface in Fig. A.1(b). At this take-off angle, Ga-As/(Ga-As+Ga-O) is 0.52 for the 1-hour annealed interface with the adjusted d_{GaAs}, which is larger than the result for the 1-min. annealed interface (0.35). The observed difference in Ga-As/(Ga-As+Ga-O) reveals the intrinsic effects of annealing on the HAXPES spectra.

B. Supplementary material

Supplemantary material associated with this article is provided.

CRediT authorship contribution statement

Naoteru Shigekawa: Conceptualization of this study, Writing- Original draft preparation, Project administration, Supervision. **Ryo Kozono:** Investigation, Formal analysis. **Sanji Yoon:** Methodology, Investigation, Formal analysis. **Tomoya Hara:** Investigation, Formal analysis. **Jianbo Liang:** Methodology, Resources. **Akira Yasui:** Resources.

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Supplementary material

Effects of post bonding annealing on GaAs//Si bonding interfaces and its application for sacrificial-layer-etching based multijunction solar cells

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Effects of post-bonding annealing on resistance across n⁺-GaAs//n⁺-Si interfaces fabricated by SAB with substrate heating at 200 °C

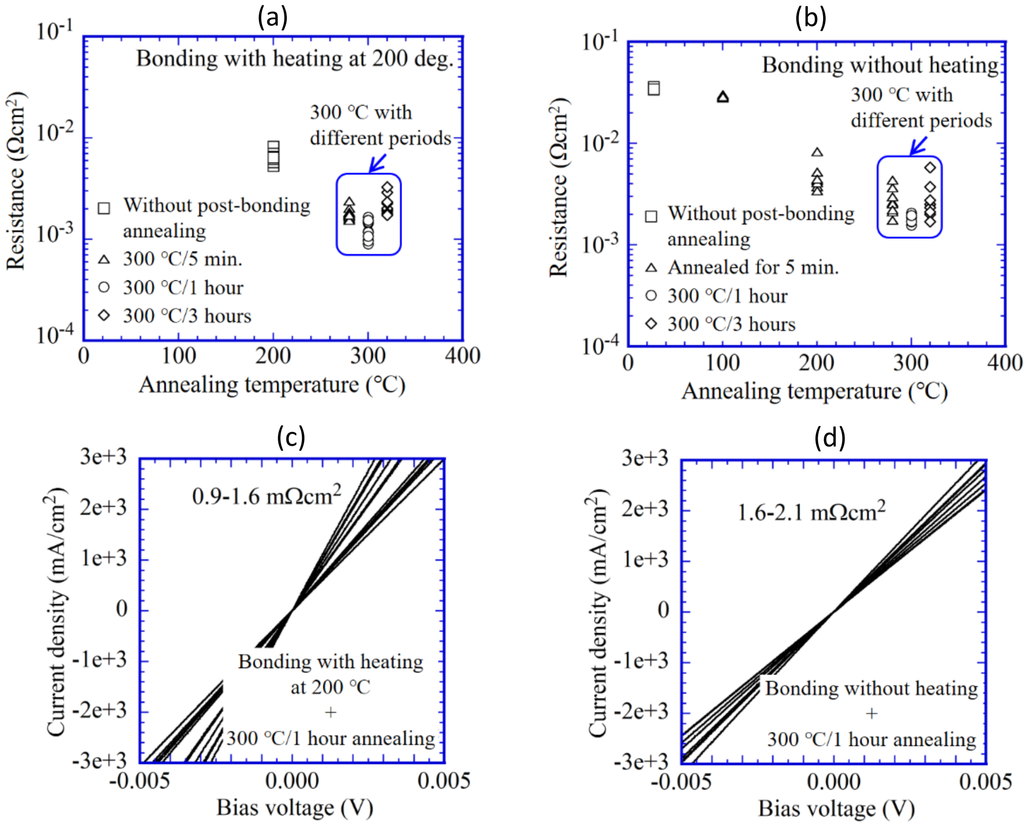

Figure S1: Relationship between annealing temperature/period and resistance of (a) n⁺-GaAs//n⁺-Si junctions fabricated by SAB with substrate heating at 200 °C and (b) junctions fabricated by SAB without substrate heating. (b) is the same as Fig. 6. Although the data are scattered, the lowest resistance in (a) (0.9~1.6 mΩcm²) is slightly smaller than that in (b) (1.6~2.1 mΩcm²). I-V characteristics of the two types of junctions annealed at 300 °C for 1 hour are shown in (c) and (d) for reference.

Characteristics of 1J GaAs cell bonded to n⁺-Si substrate fabricated using the SL-etching approach.

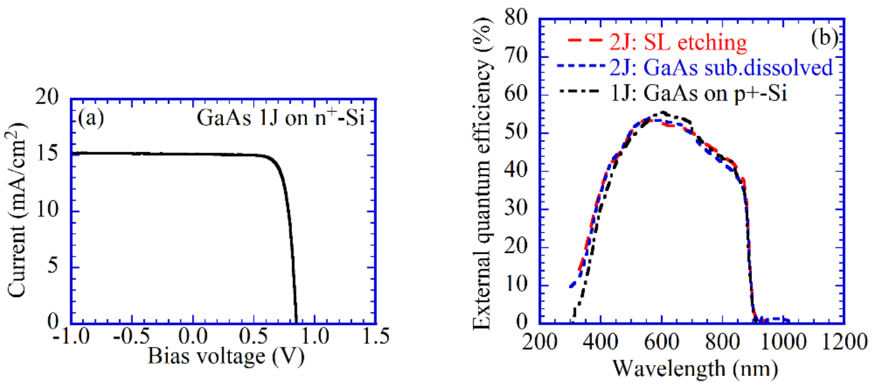

Figure S2: (a) I-V characteristics under the AM1.5G/one sun solar irradiance and (b) EQE spectra of a 1J GaAs cell//n⁺-Si substrate fabricated using the SL etching. EQE of GaAs subcell of two 2J (Fig. 7(b)) is also shown in (b) for comparison. The short-circuit current of GaAs 1J cell (15.1 mA/cm² from (a)) is comparable to the integration of EQE of GaAs subcells in GaAs/Si 2J (Table 1). EQE of GaAs 1J is quite similar to that of GaAs subcells in 2J.